DIGITAL

LOGIC

(6)

Digital Logic

PUSHP

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DIGITAL ELECTRONICS

1) Minimization And Logical Expression
   A) Boolean Algebra
   B) K-Map

2) Logic Gate.
   - Half Adder
   - Half Substractor
   - Full Adder
   - Full Substractor
   - PA
   - LAC

3) Combinational Gate.
   - MUX
   - DeMUX
   - Decoder
   - Encoder
   - Comprator
   - Code Converter

4) Sequential circuit
   - Flip-Flop
   - Register
   - Counter

5) Number System, Codes, Data Representation.

6) ADC / DAC

7) Logic family

8) Semiconductor Memories.

References:-

Digital Logic Design — M. Manno

Logic Design → Roth

Digital integrated Electronic — Taub & Schilling.

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Minimization And Logic Expression.

→ Boolean Algebra is used when number of variables are less & o/p may be 0 & 1.

→ K-map is used 5 variable and output 0, 1, X

→ Tabulation method is used when no. of variables are more

☆ Boolean Algebra :→

Switch → ON → 1
→ OFF → 0

1 NOT :→

$A \rightarrow \bar{A}$ or A'

$\bar{A} \rightarrow A$

2. AND :→

$0 \cdot 0 = 0$ $\quad A \cdot A = A$

$0 \cdot 1 = 0$ $\quad A \cdot 0 = 0$

$1 \cdot 0 = 0$ $\quad A \cdot 1 = A$

$1 \cdot 1 = 1$ $\quad A \cdot \bar{A} = 0$

3 OR :→

$A + A = A$

$A + 0 = A$

$A + 1 = 1$

$A + \bar{A} = 1$

A	B	y
0	0	0
0	1	1
1	0	1
1	1	1

Q $AB + A\bar{B}$

Sol: $= A(B + \bar{B})$

$= A$

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Q. $AB + A\bar{B}C + A\bar{B}\bar{C}$ Then minimum no. of NAND gate is

a) 0 b) 1 c) 2 d) 3

Sol: $AB + A\bar{B}C + A\bar{B}\bar{C}$

$= AB + A\bar{B}(C + \bar{C})$

$= AB + A\bar{B}$

$= A(B + \bar{B})$

$= A$.

∴ Minimum no. of gate = 0

∴ (a) Ans.

⇒ Advantages of Minimization :→

i) Number of logic gates decreases.
ii) Speed of operation will increased
iii) Power dessipation will reduced
iv) Complexity of circuit is less.
v) Fan in may be reduces.

Q. $A\bar{B} + AB\bar{C} + A\bar{B}\bar{C}D$

Sol: $A\bar{B} + AB\bar{C} + A\bar{B}\bar{C}D$

$= A\bar{B}(1 + \bar{C}D) + AB\bar{C}$

$= A\bar{B} + AB\bar{C}$

$= A(\bar{B} + B\bar{C})$

$= A(\bar{B} + \bar{C})$ [$\because \bar{B} + B\bar{C} = \bar{B} + \bar{C}$]

→ $(A + B)(A + C) = A + BC$ → Transposition.

$= A + AC + AB + BC$

$= A[1 + C + B] + BC$

$= A + BC$

Q. $(\bar{x} + y)(\bar{x} + z) = ?$ $\bar{x} + yz$ Ans.

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Q: $(A+B+C)(A+\bar{B}+C)(A+B+\bar{C})$

Sol: $(A+B+C)(A+\bar{B}+C)(A+B+\bar{C})$

$= (A+B+C\bar{C})(A+\bar{B}+C)$

$= (A+B)(A+\bar{B}+C)$

$= A + B(\bar{B}+C)$

$= A + BC$ Ans.

Q: $(A+B)(A+\bar{B})(\bar{A}+B)(\bar{A}+\bar{B})$

Sol: $= (A+B\bar{B})(\bar{A}+B\bar{B})$

$= A \cdot \bar{A} = 0$ Ans.

→ $A + BC = (A+B)(A+C)$

① + ②③ ① + ② ① + ③

→ $A + \bar{A}B = (A+\bar{A})(A+B) = A+B$.

→ $A + \bar{A}\bar{B} = (A+\bar{A})(A+\bar{B}) = A+\bar{B}$

→ $\bar{A} + AB = (\bar{A}+A)(\bar{A}+B) = \bar{A}+B$.

→ $\bar{A} + \bar{A}\bar{B} = \bar{A} + \bar{B}$

Q: $AB + \bar{A}\bar{B} + A\bar{B}$

Sol: $AB + \bar{A}\bar{B} + A\bar{B}$

$= A(B+\bar{B}) + \bar{A}\bar{B}$

$= A + \bar{A}\bar{B}$

$= A + \bar{B}$ Ans.

Q: $AB + \bar{A}B + A\bar{B}$

Sol: $= A(B+\bar{B}) + \bar{A}B$.

$= A + \bar{A}B = A + B$ Ans.

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Q $AB\bar{C} + ABC + \bar{A}BC$

Sol: $AB\bar{C} + ABC + \bar{A}BC$

$= AB(C+\bar{C}) + \bar{A}BC$

$= AB + \bar{A}BC$

$= B(A+\bar{A}C)$

$= B(A+C)$

$= AB + BC$ Ans

2nd Method:

$AB\bar{C} + ABC + \bar{A}BC$

$AB(C+\bar{C}) + BC(A+\bar{A})$

$AB + BC$ Ans.

☆ Consensus or Redancy Theorem:→

$AB + \bar{A}C + BC = AB + \bar{A}C$

Proof:

$AB + \bar{A}C + BC$

$= AB + \bar{A}C + BC(A+\bar{A})$

$= AB + \bar{A}C + ABC + \bar{A}BC$

$= AB(1+C) + \bar{A}C(1+B)$

$= AB + \bar{A}C$ Proved.

→ Three variables

→ Each variables used two times.

→ One variable is complemented / uncomplemented.

→ It is also called Sum of product

Q $AB + B\bar{C} + AC$

Sol: $AB + B\bar{C} + AC = B\bar{C} + AC$ Ans.

Q. $A\bar{B} + Bc + AC$

Sol: $A\bar{B} + Bc + AC = A\bar{B} + Bc$ Ans.

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☆ Product of sum (POS) :→

$(A+B)(\bar{A}+C)(B+C)$

$= (\bar{A}+C)(A+B)$

Q. $(A+B)(\bar{B}+C)(A+C)$

$= (\bar{B}+C)(A+B)$

Q. $\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C}$

Sol: $\bar{A}\bar{B} + A\bar{C}$

Q $\bar{A}\bar{B} + \bar{B}C + \bar{A}\bar{C}$

$\bar{B}C + \bar{A}\bar{C}$

Q. $(\bar{A}+\bar{B})(\bar{B}+\bar{C})(\bar{A}+C)$

$(\bar{A}+C)(\bar{B}+\bar{C})$ Ans.

☆ Demorgan's Theorem :→

$$\overline{A\,BC} = \bar{A}+\bar{B}+\bar{C}$$

$$\overline{A+B+C} = \bar{A}\,\bar{B}\,\bar{C}$$

→ Boolean Algebra :→

1) Minimization.
2) SOP → Minimal, Canonical
3) POS → Minimal, Canonical
4) Dual
5) Complement expression.
6) Truth table
7) Venn diagram
8) Switching circuit
9) Statement

1) Minimisation :→

Q. $XY + X\bar{Y}$ WIZ.
$A + \bar{A}B$.

Sol: $= XY + WZ$ Ans.

Q. Let $f(A,B) = \bar{A} + B$. then the value of $f(f(x+y, \bar{y}), z)$ is
a) $xy + z$ b) $x\bar{y} + z$ c) $\bar{x}y + z$ d) x

Sol: $f(x+y, \bar{y}) = \overline{x+y} + y$ $[\because f(A,B) = \bar{A} + B]$
$= \bar{x} \cdot \bar{y} + y$
$= \bar{x} + y$
$f(\bar{x}+y, z) = \overline{\bar{x}+y} + z$ $[\because f(A,B) = \bar{A} + B]$
$= x\bar{y} + z = f(f(x+y, y), z)$.

Q. Let $x * y = \bar{x} + y$ & $z = x * y$ then the value of $z * x$ is
a) x b) 1 c) 0 d) $\bar{x}$

Sol: $x * y = \bar{x} + y$ } given.
$z = x * y$

$\therefore z = x * y = \bar{x} + y$

$z * x = \bar{z} + x$
$= \overline{\bar{x}+y} + x$
$= x\bar{y} + x$
$= x(1+\bar{y})$
$= x$ Ans.

2) Sum of Product (SOP) :—

$ABC + \bar{A}BC + (A\bar{B}C)$ → Product term.

In SOP form each product term is known as min term or implement. It is used when O/P of logical expr. is 1.

Ex 5 → 101
$A\bar{B}C$

9 → 1001
$AB\bar{C}D$.

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Q. For the given truth table minimise SOP expression.

Sol:

	A	B	Y	Min term
0	0	0	1	$\bar{A}\bar{B}$
1	0	1	0	
2	1	0	1	$A\bar{B}$
3	1	1	0	

$Y = \bar{A}\bar{B} + A\bar{B}$

$= \bar{B}(A+\bar{A})$

$= \bar{B}$ Ans.

$Y(A,B) = \Sigma m(0,2)$

Q. Simplified the expression for $Y(A,B) = \Sigma m(0,2,3)$

Sol: $Y(A,B) = \Sigma m(0,2,3)$

$= \bar{A}\bar{B} + A\bar{B} + AB$

$= A(B+\bar{B}) + \bar{A}\bar{B}$

$= A + \bar{A}\bar{B}$

$= A + \bar{B}$ Ans

→ SOP → Minimal $A+B$.

→ Canonical

$A \cdot 1 + \bar{A}B$

$A(B+\bar{B}) + \bar{A}B$

$AB + A\bar{B} + \bar{A}B$

In canonical SOP or standered SOP form each minterm contain all variable.

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Q. In canonical SOP form the number of min term in logical expression, $A + \bar{B}C$ is

a) 4 b) 5 c) 6 d) 7.

Sol: $A + \bar{B}C = A(B+\bar{B})(C+\bar{C}) + \bar{B}\bar{C}(A+\bar{A})$

$= A[BC + B\bar{C} + \bar{B}C + \bar{B}\bar{C}] + A\bar{B}C + \bar{A}\bar{B}C$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$

$= 5$ min term.

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☆ Product of Sum (POS) :→

$(A+B+\bar{C})(\bar{A}+B+\bar{C})(A+B+C)$

↳ Max term.

POS form are used when O/P is logic 0

Ex → 5 → 101.

$\bar{A}B\bar{C}$

Q. For the given truth table minimise POS expression :-

A	B	Y	MAX term
0	0	1	
0	1	0	$(A+\bar{B})$
1	0	1	
1	1	0	$(\bar{A}+\bar{B})$

$Y(A,B) = (A+\bar{B})(\bar{A}+B) = A\bar{A}+AB+\bar{A}\bar{B}+B\bar{B}$

$= \bar{B}$

$Y(A,B) = \pi M(1,3) = \bar{B}$

$\therefore Y(A,B) = \Sigma m(0,2) = \bar{B}$

$\Sigma m(0,2) = \pi M(1,3)$

Note :—

→ With n variable max^m possible min term are max term 2^n.

AB → 16

AB	$A\bar{B}$	A	1
$A+B$	$\bar{A}B$	$\bar{A}$	0
$\bar{A}\bar{B}$	$A+\bar{B}$	B	$\bar{A}B+A\bar{B}$
$\bar{A}+\bar{B}$	$\bar{A}+B$	$\bar{B}$	$AB+\bar{A}\bar{B}$

→ With n variables max^m possible logical expression are 2^{2^n}

for n = 2 $2^{2^2} = 6$

= 3 $2^{2^3} = 256$

= 4 $2^{2^4} = 2^{16} = 2^6 \times 2^{10} = 64K$

$= 65536$

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☆ Dual :→

+Ve logic	-Ve logic
Logic 0 → 0V	Logic 0 = +5V
Logic 1 → +5V	Logic 1 = 0V

Ex :-

→ Logic 0 → -5V ⟶ +Ve Logic.
Logic 1 → 0V

→ ECL :-

Logic 0 → -1.7V ⟶ +Ve Logic.
Logic 1 → -0.8V

→ +Ve Logic AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

-Ve Logic OR

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

+Ve Logic OR.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

+Ve Logic AND = -Ve Logic OR
-Ve Logic AND = +Ve Logic OR.

→ Dual expression is used +Ve logic to -Ve logic and -Ve logic to +Ve logic.

→ STEPS :→

1) AND ↔ OR
   . ↔ +
2) 1 ↔ 0
3) Keep Variable as it is

→ For any logical expression if two times dual is used result is same expression.

Q. Write dual expression of the following expression.
$A\bar{B}\bar{C} + \bar{A}BC + ABC$

Sol:- $A\bar{B}\bar{C} + \bar{A}BC + ABC$

$(A+\bar{B}+\bar{C}) \cdot (\bar{A}+B+C) \cdot (A+B+C)$ Ans.

$A\bar{B}\bar{C} + \bar{A}BC + ABC$

☆ Self Dual :→

$AB + BC + AC$

$= (A+B)(B+C)(\bar{A}+C)$

$= (B+AC)(A+C)$

$= AB + BC + AC$

→ In self dual expression if one time dual is used resulting in same expression.

→ In n-variables, max^m possible dual expression is,

$$\text{Max}^m \text{ possible dual Expression} = 2^{2^{n-1}}$$

For n = 1 2

= 2 4

= 3 16

☆ Complement :→

→ Steps :-

1) AND ↔ OR

2) 1 ↔ 0

3) Complement each variables.

Q $Y = ABC + \bar{A}BC + A\bar{B}C$

$\bar{Y} = (\bar{A}+\bar{B}+\bar{C})(A+\bar{B}+\bar{C}) \cdot (\bar{A}+B+\bar{C})$ Ans

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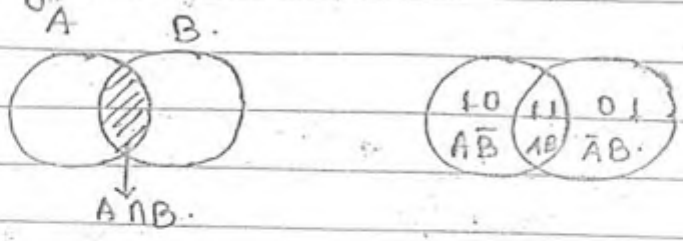
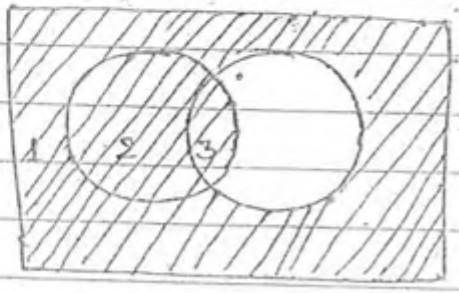
☆ Venn Diagram :→



Q. For the given Venn diagram, minimise SOP expression for shaded areas.



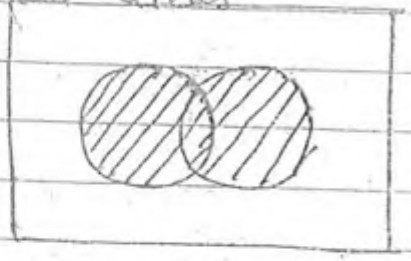
Sol: $\bar{A}\bar{B} + A\bar{B} + AB$

$= A(B+\bar{B}) + \bar{A}\bar{B}$

$= A + \bar{A}\bar{B}$

$= A + \bar{B}$ Ans

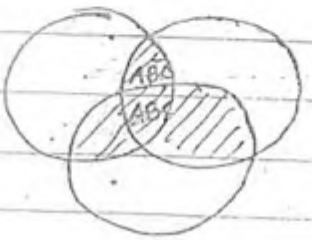
Q. For the given Venn diagram, minimise the expression for shaded areas.



Sol: $A\bar{B} + AB + \bar{A}B$

$A(B+\bar{B}) + \bar{A}B = A + \bar{A}B = A + B.$

Q.



$ABC + AB\bar{C} + A\bar{B}C + \bar{A}BC$

$AB[C+\bar{C}] + AC[B+\bar{B}] + BC[A+\bar{A}]$

$AB + AC + BC$

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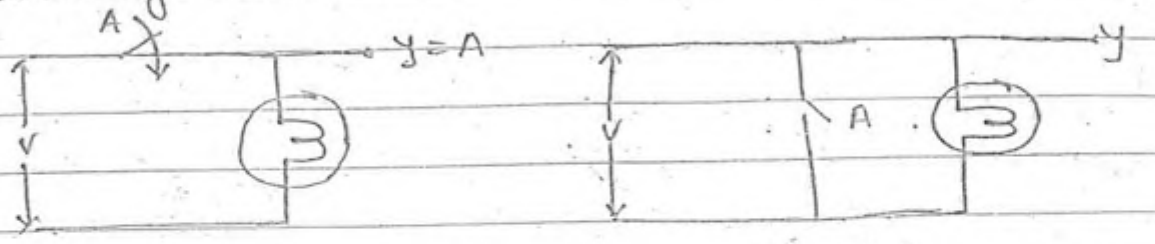
✡ Switching Circuit :→

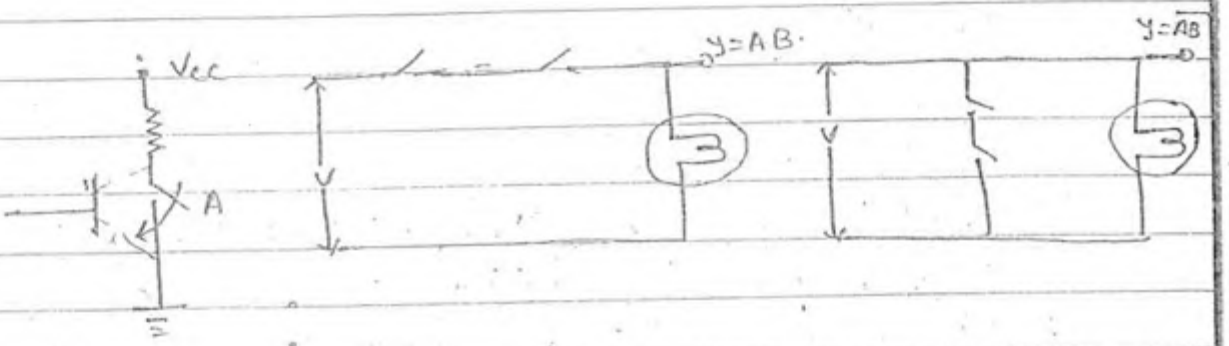


Series.

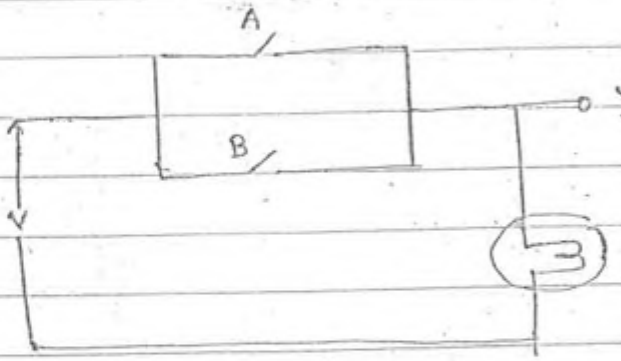
Parallel.

A	y
0	0
1	1

A	y
0	1
1	0

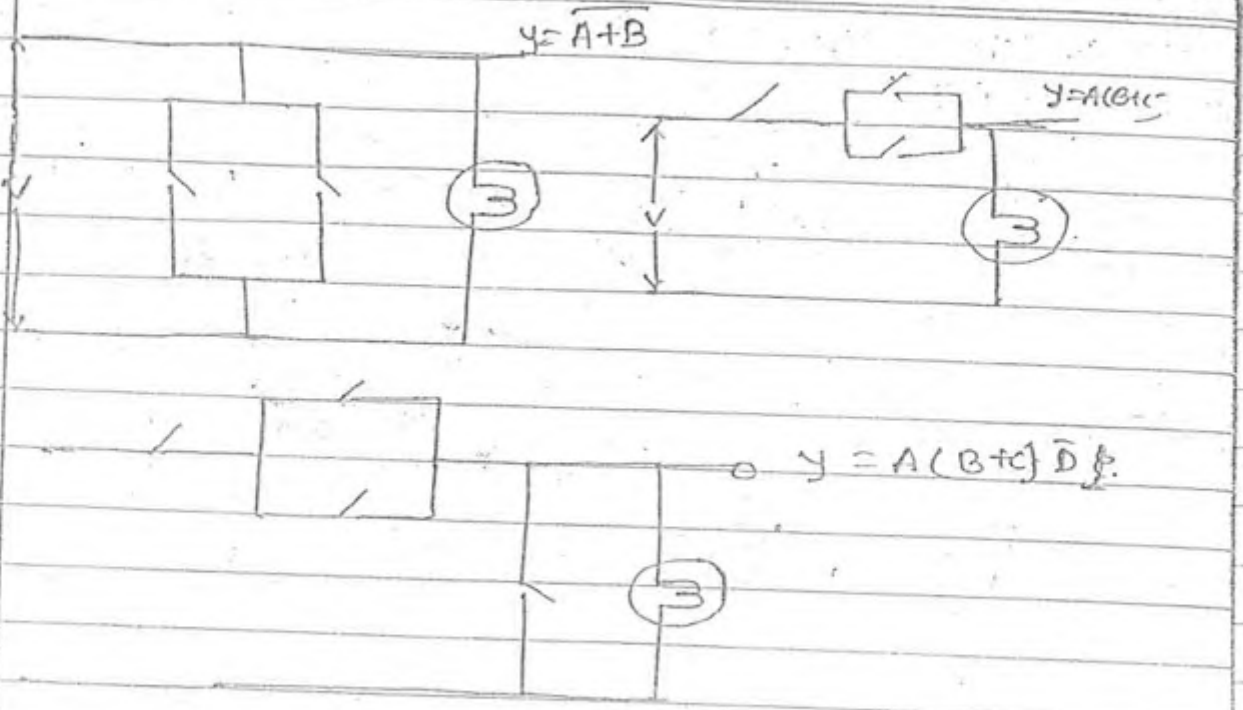


A	y
0	1
1	0



A	B	y
0	0	1
0	1	1
1	0	1
1	1	0 → Maxterm

$\bar{A}+\bar{B} = \overline{AB}$



Statements :→

Q. In logic circuit have three I/P, A, B, C and O/P is Y. Y is 1 for the following combinations.

i) B and C are true → $B\bar{C}$

ii) A and C are false → $\bar{A}\bar{C}$

iii) A, B and C are true → ABC

iv) A, B and C are false → $\bar{A}\bar{B}\bar{C}$

Then minimise the expression for Y.

Sol: $Y = B\bar{C} + \bar{A}\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$

$= BC(1+A) + \bar{A}\bar{C}(1+\bar{B})$

$= BC + \bar{A}\bar{C}$

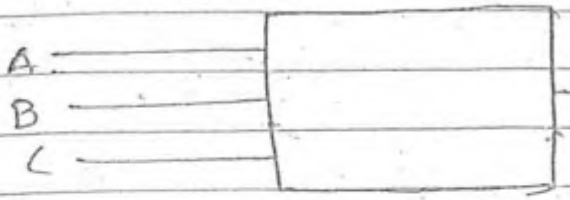
Q. A logic circuits have three I/P, A, B, C & O/P is F. F is 1 When majority no. of I/P are at logic 1.

i) Minimise the expression for F

ii) Implement logic circuit.

Sol:

4



A	B	C	F	Min term.
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\bar{A}BC$
1	0	0	0	
1	0	1	1	$A\bar{B}C$
1	1	0	1	$AB\bar{C}$
1	1	1	1	ABC

$$F = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= AB + BC + AC$$

→ 11 11 11.

* Logic Gates :→

Basic building blocks.

NOT
OR
AND
→ Basic gate.

NAND
NOR
→ Universal gate.

EXOR
EXNOR
→ Arithmetic Ckt
Comprator
Parity generator / Checkers.
Code converter.

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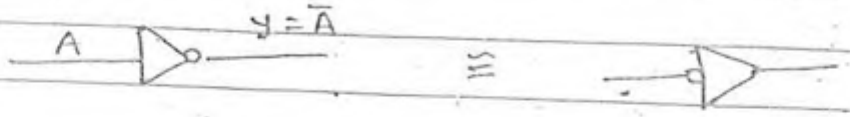
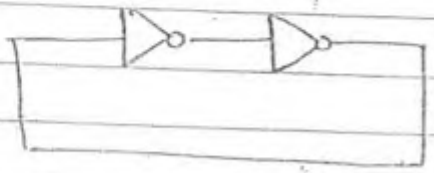
1. NOT :→



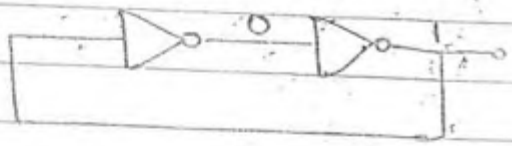
A	Y
0	1
1	0

Q The circuit shown in figure.

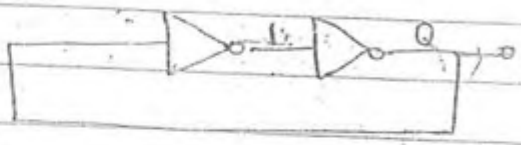


a) Buffer (When we apply theni o/p is obtained)
b) Astable Multivibrator
c) Bistable Multivibrator
d) Square wave generator.

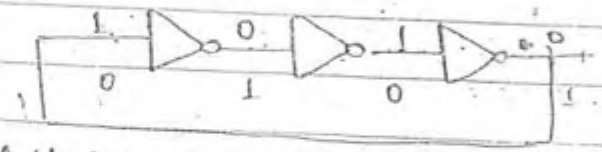
Sol:

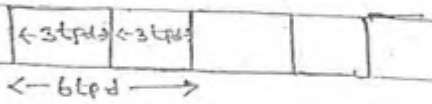


Basic Memory
Bistable multivibrator



Q.





a) Astable Multivibrator
b) Square wave generator
c) Clock generator
d) Ring oscillator.

$T = 6t_{pd}$.
$= 2 \times 3 t_{pd} = 2Nt_{pd}$.
N = No. of inverter

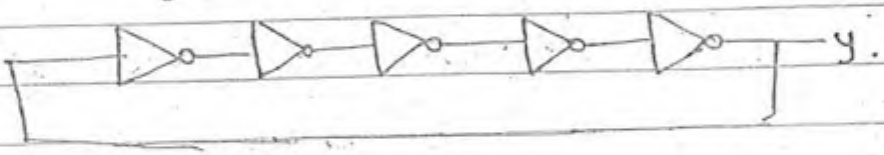
→ In ring oscillator, $\boxed{T = 2Nt_{pd}}$.

When N = No. of inv in feedback

Q The circuit shown in figure, propagation delay of each NOT gate is 100 ps then frequency of square wave is

a) 10 GHz b) 1 GHz c) 50 GHz d) 5 GHz.

Sol:



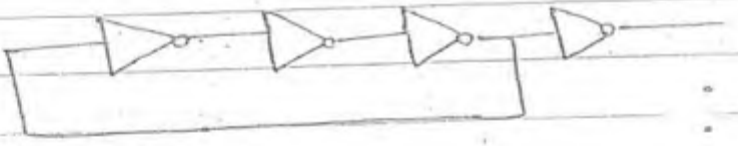
Sol: $T = 2Nt_{pd}$

$= 2 \times 5 \times 100 \times 10^{-12} = 10^{-9}$

$f = \frac{1}{T} = 10^{9} = 1\,GHz$ Ans.

Q. The circuit shown in figuit, propagation delay of each NOT gate is 2ns, then time period of generated Squarewave

a) 6 b) 12 c) 14 d) 16



Sol: $T = 2Nt_{pd}$

$= 2 \times 3 \times 2 = 12$

2 AND Gate :→

$Y = AB$.

→ Truth Table :-

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

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→ Commutative Law:-

$$AB = BA$$

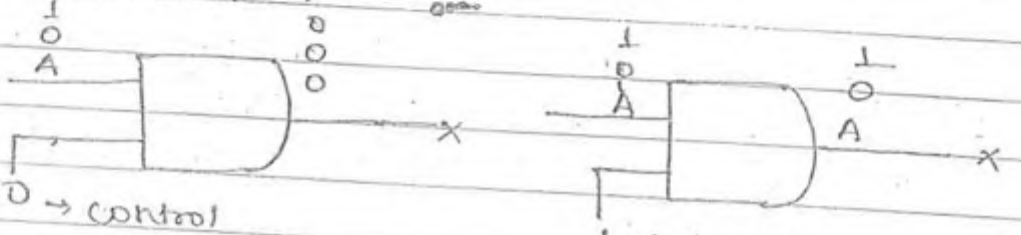
→ Associative Law:→

$$ABC = (AB)C = A(BC)$$

Note:→

* AND gate follows commutative as well as associative law.
* AND gate is series switches.

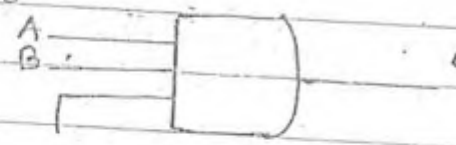
→ Enable / Disable :→



O/P not change
∴ Disable

I/O changes.
∴ Enables.

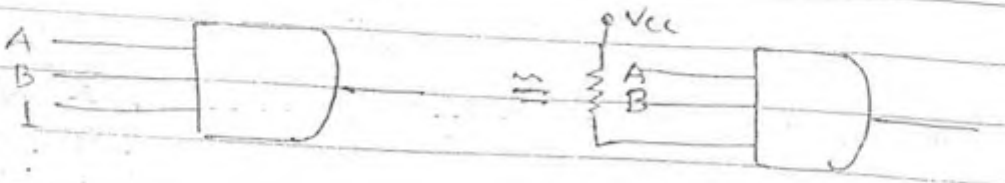
→ In TTL logic family open or floating I/P will act as logic 1 where as in ECL, I/P will act as logic '0'



Open or floating I/P.

→ In multi I/P AND gate unused I/P can be connected

A) Logic 1 or Pull up:-



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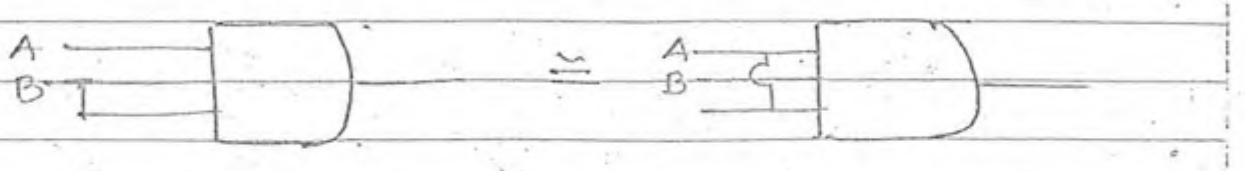
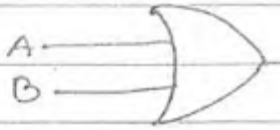
B) Connected to one of one I/P :-



C) If it is TTL logic family then unused I/P can be open or float

D) Best way of connecting unused I/P of AND gate is connected to logic 1.

3 OR Gate :→

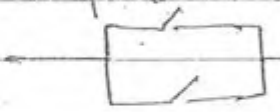


$Y = A+B$.

→ Truth table :-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

→ OR gate is parallel switch.



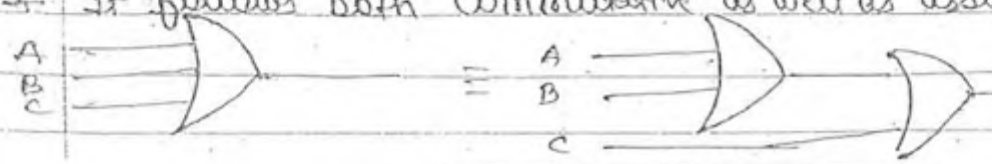
→ Commutative law :-

$A+B = B+A$.

→ Associative Law :→

$A+B+C = (A+B)+C$.

→ It follows both commutative as well as associative law.



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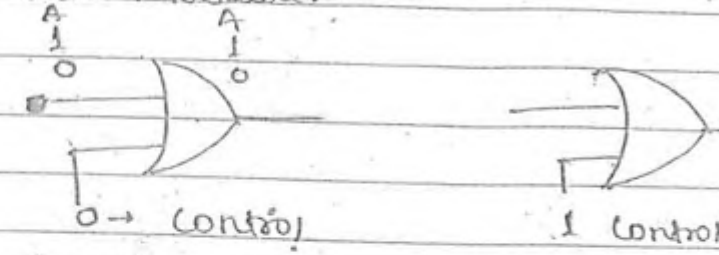
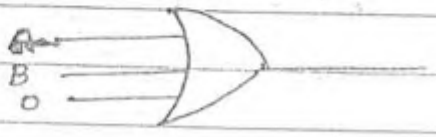
→ Enable / Disable :→

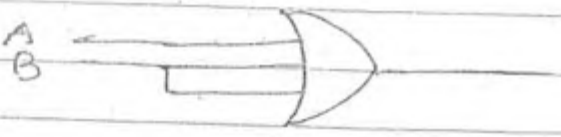


→ In multi I/P OR gate, unused I/P can be connected

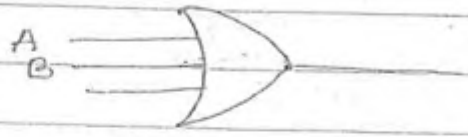
A) Logic '0' or Pull Down :-



B) One of used I/P



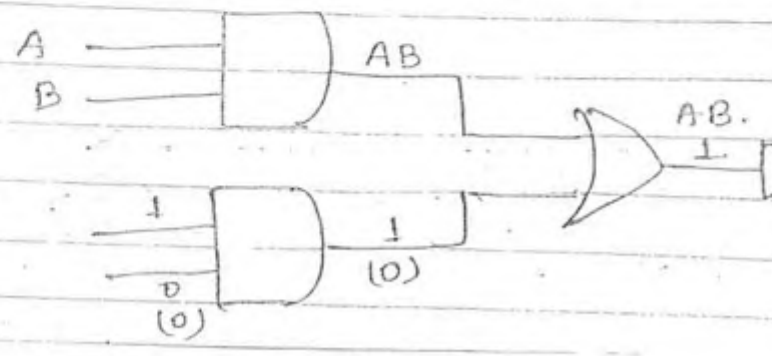
C) If it is ECL, then unused I/P can be Open / float.



Oct-2004

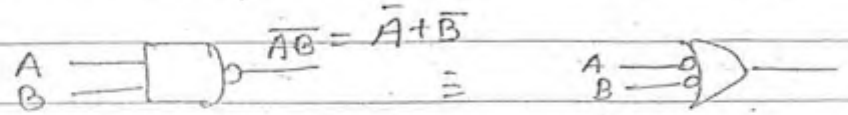
Q. The circuit shown in figure is TTL AND-OR inverter then for the given I/P, O/P is

a) 0 b) 1 c) AB d) $\overline{AB}$

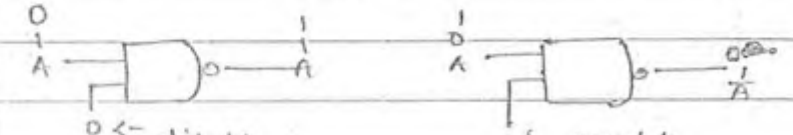


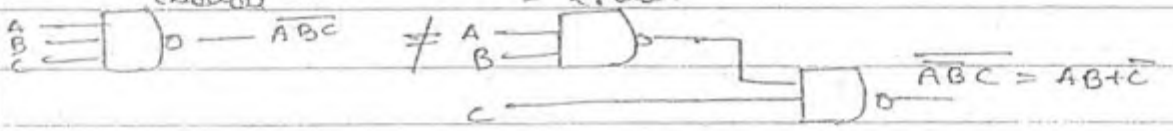
for ckt in ECL
Any is (....) → ✗

4. NAND Gate :→

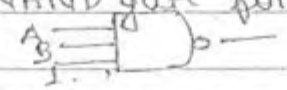


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



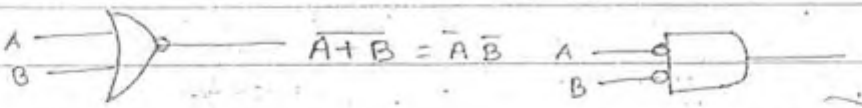


NAND gate follows associative law but not follow commutative law



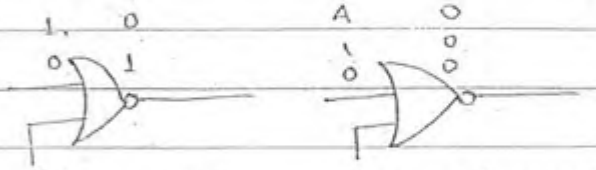
Unused I/P of a NAND gate can be connected similar to unused I/P of a AND gate.

5 NOR Gate :→



Bobbled AND

A	B	Y
0	0	1
0	0	0
1	0	0
1	1	0



It follows commutative law but not associative law

→ Commutative Law :-

$\overline{A+B} = \overline{B+A}$

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→ Associative law: →

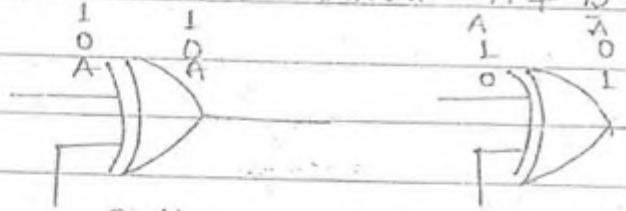
$\overline{A+B+C} \neq \overline{\overline{A+B}+C}$

→ Unused I/P of NOR gate can be connected similar to OR gate

6 EXOR or XOR gate (: Exclusive OR gate) :→

A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

In XOR gate O/P is 0 when $A = B \Rightarrow y = 0$
When O/P is 1 when $A \neq B \Rightarrow y = 1$



0 Buffer Enable

1. Inverter

It is also called Controlled inverter.

$A \oplus A = 0$

$A \oplus \bar{A} = 1$

$A \oplus 0 = A$

$A \oplus 1 = \bar{A}$

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Q If $A \oplus B = C$ then $A \oplus C = ?$

Sol: $A \oplus C = B$

$B \oplus C = A$

$A \oplus B \oplus C = 0$

→ $A \oplus A = 0$

$A \oplus A \oplus A = A$

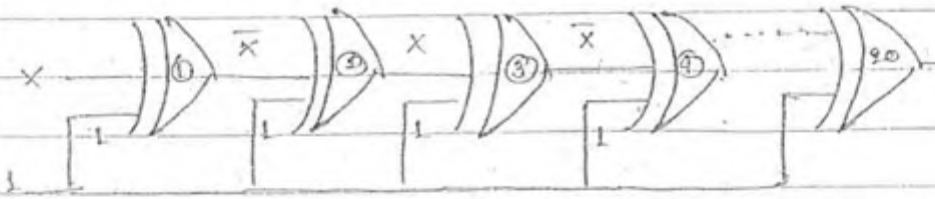
$A \oplus A \oplus A \oplus A = 0$

→ $B \oplus B \oplus B \oplus \cdots$ n terms.

$= B$ When n is odd

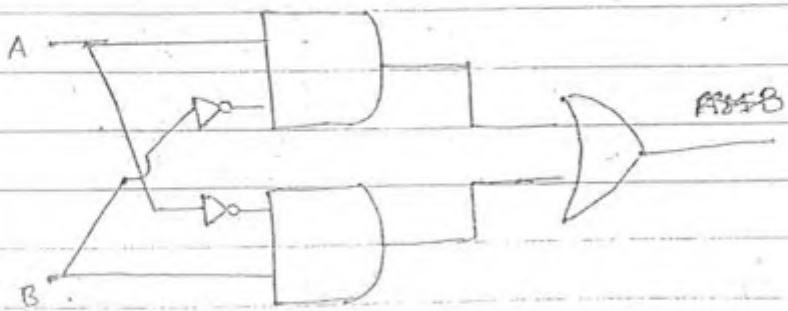
$= 0$ When n is even.

Q. The ckt shown in figure contains cascading of XOR gate for given I/P, O/P Y is a) 1 b) 0 c) x d) $\bar{x}$



D

Q



→ XOR gate follows both commutative or associative law.

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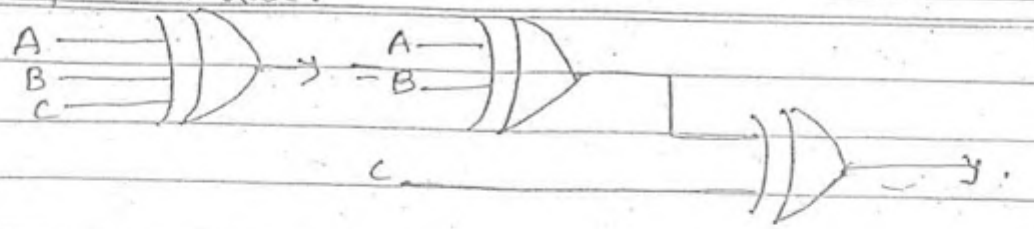
→ 3 I/P XOR Gate :→



A	B	y	
0	0	0	
0	1	1	✓
1	0	1	✓
1	1	0	

→ In x-OR gate O/P is 1 when no of 1's at I/P = odd number

→

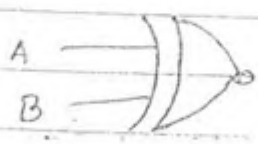
A	B	C	Y = A ⊕ B ⊕ C.	
0	0	0	0	
0	0	1	1	✓
0	1	0	1	✓
0	1	1	0	
1	0	0	1	✓
1	0	1	0	
1	1	0	0	
1	1	1	1	✓

$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

001 010 100 111 → odd no of 1's.

$= \Sigma m(1, 2, 4, 7)$

7 EXNOR or XNOR [Exclusive NOR Gate] :→



A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

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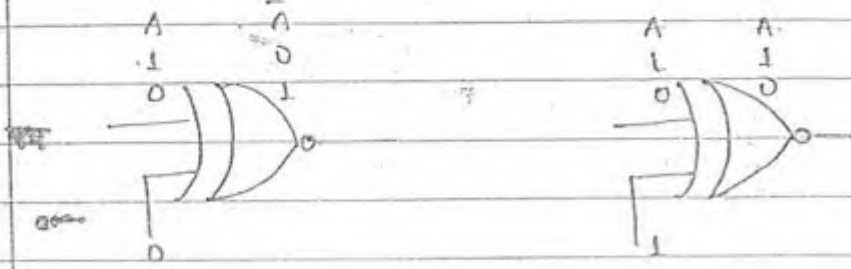
SOP → $\bar{A}\bar{B} + AB$.

POS → $(A+B)(\bar{A}+B)$

O/P is 1 when $A = B \Rightarrow 1$. Coincedence logic ckt
Equivalence detector

O/P is 0 when $A \neq B$

→



Inverter Buffer

$A \odot A = 1$
$A \odot \bar{A} = 0$
$A \odot 0 = \bar{A}$
$A \odot 1 = A$

☆ Comparision Between XOR & XNOR :-

$A \oplus A = 0$	$A \odot A = 1$
$A \oplus A \oplus A = A$	$A \odot A \odot A = A$
$A \oplus A \oplus A \oplus A = 0$	$A \odot A \odot A \odot A = 1$

→ $A \oplus B = \overline{A \odot B}$
$A \oplus B \oplus C = A \odot B \odot C$
$A \oplus B \oplus C \oplus D = \overline{A \odot B \odot C \odot D}$

XOR & XNOR are not complement to each other, when number of I/P are odd.

$(A \odot B) \odot C = (\bar{A}\bar{B} + AB) \odot C$
$(\overline{\bar{A}\bar{B} + AB})\bar{C} + (\bar{A}\bar{B} + AB)C$
$(\bar{A}B + A\bar{B})\bar{C} + \bar{A}\bar{B}C + ABC$

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Q For the given truth table the logical expression is

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$Y = \overline{A \oplus B \oplus C} = \overline{A \odot B \odot C}$

a) $A \oplus B \oplus C$

b) $A \odot B \odot C$

✓ c) $\overline{A \odot B \odot C}$

d) $AB + BC + AC$

Imp

→ XNOR gate is even no of 1's detector when no. of I/P are even

→ XNOR gate is odd no of 1's detector when no of I/P are odd.

→ $\bar{A} \oplus B = A \odot B$.

$x \oplus y$

$\bar{x}y + x\bar{y}$

$AB + \bar{A}\bar{B}$

→ $A \odot \bar{B} = A \odot B$

$\bar{A} \odot B = A \oplus B$

$A \odot \bar{B} = A \oplus B$

→ $A \oplus B \oplus AB = A + B$

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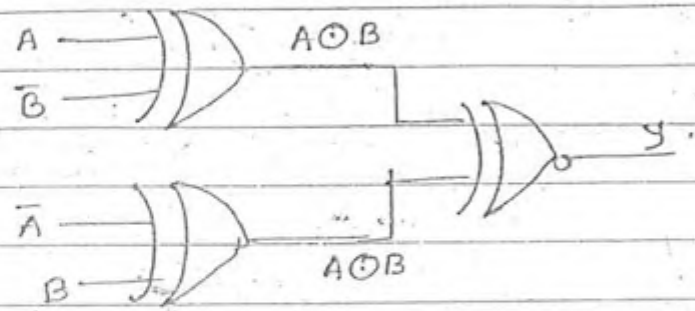
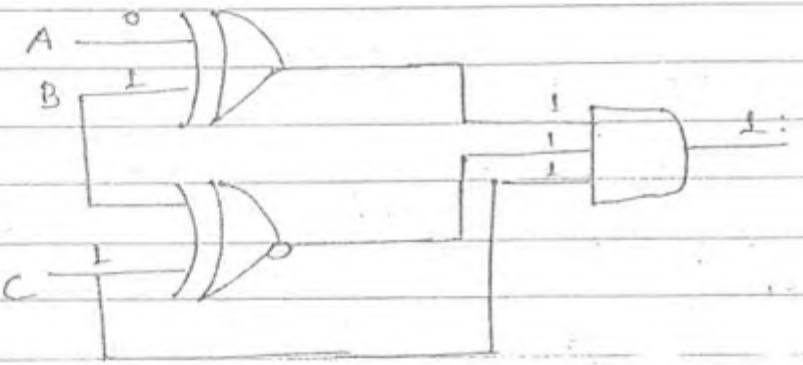
Q For the given circuit o/p y is



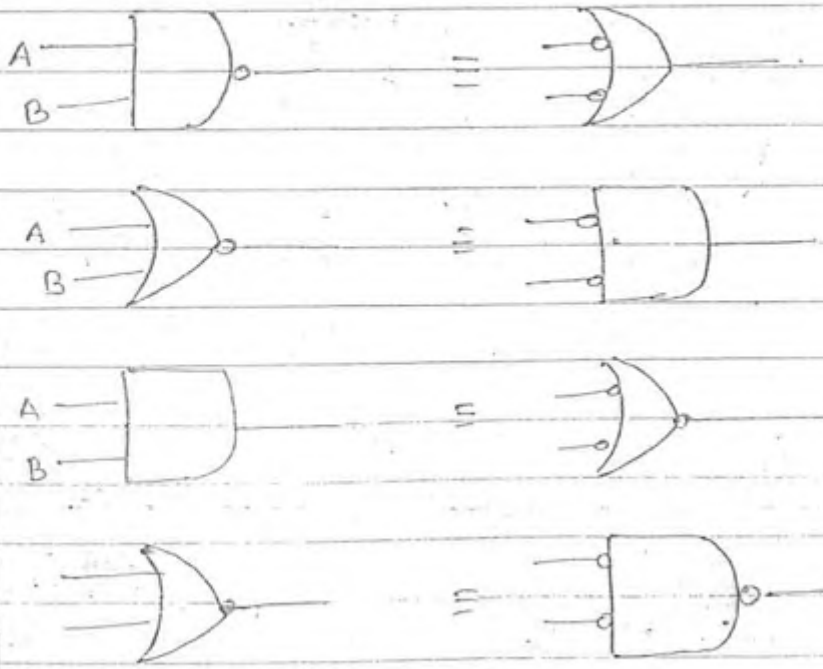
a) 0 b) 1 c) A⊕B d) A⊙B.

W.B.

Q



☆ NAND



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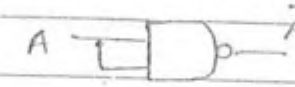
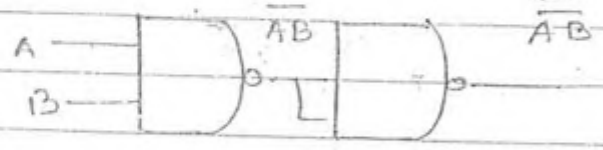
1) NAND Gate As Universal Gate :→

i) NOT :—



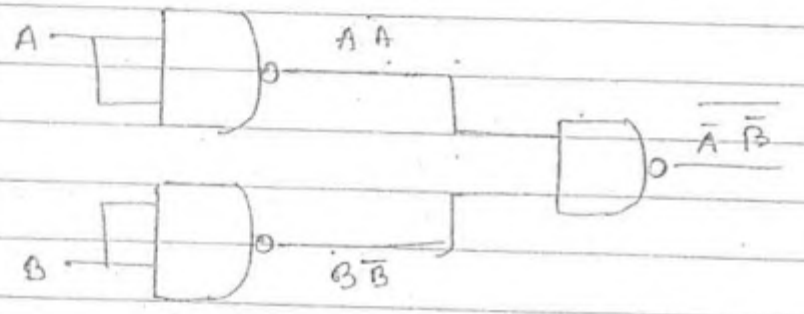
No. of Gate.
1

ii) AND :—



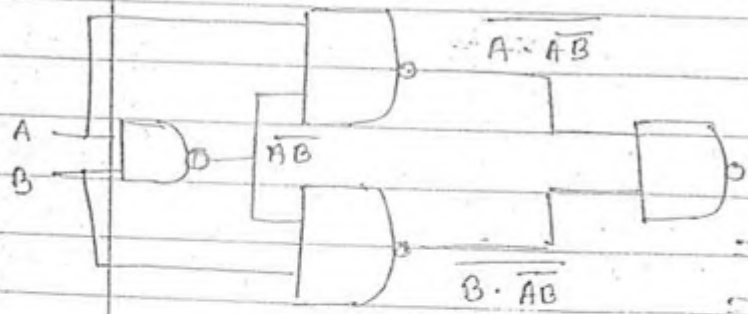
2.

iii) OR :→



3.

iv) EXOR :—



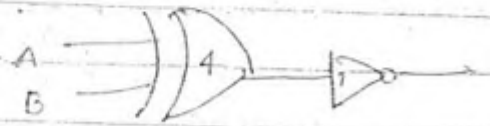
4.

$= A \cdot \overline{AB} + B \cdot \overline{AB}$

$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$

$= A\bar{B} + \bar{A}B.$

v) EXNOR :—



5

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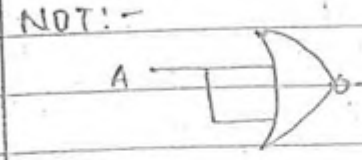
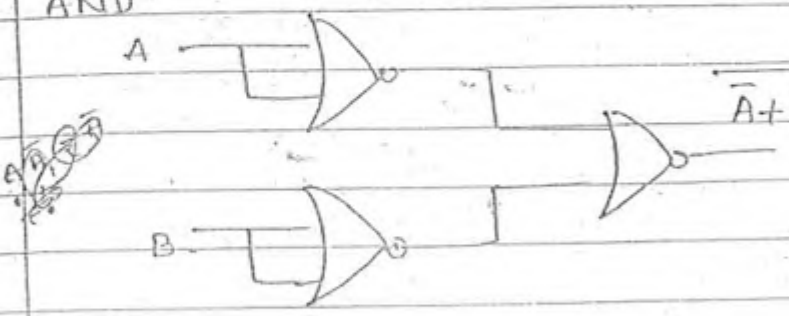
2. NOR Gate As Universal Gate :→

i) NOT :-



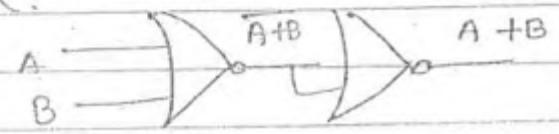
No. of gate.
1

ii) AND.



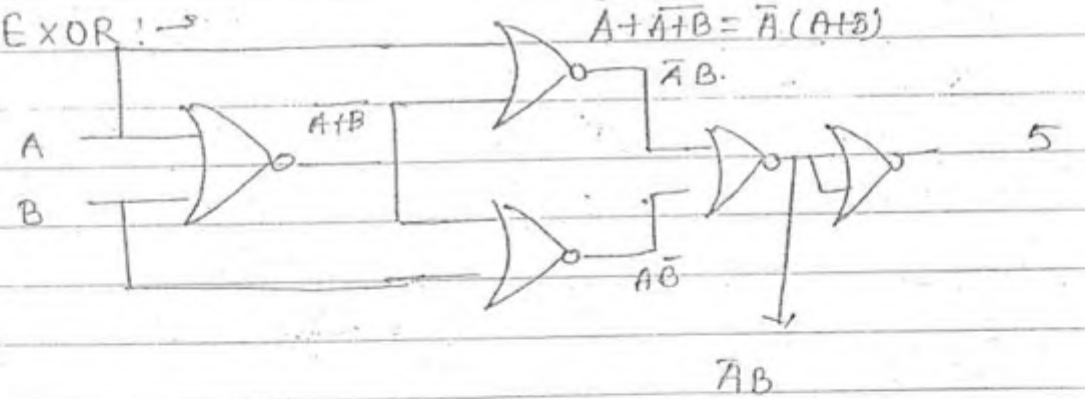
3.

iii) OR :-



2

iv) EXOR :→



5

v) EXNOR :→

vi) NAND :→

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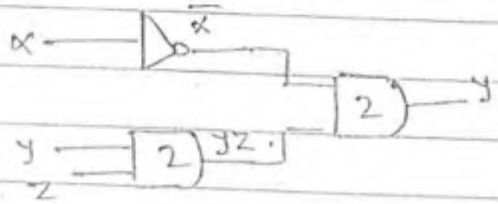
→

Logic Gate	No. of NAND	No of NOR.
NOT	1	1
AND	2	3
OR	3	2
EXOR	4	5
EXNOR	5	4

Q. To implement $\bar{x}yz$ minimum no. of two I/P NAND gate.

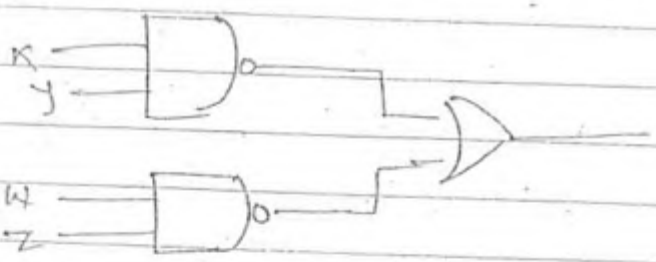
a) 3 b) 4 c) 5 d) 7

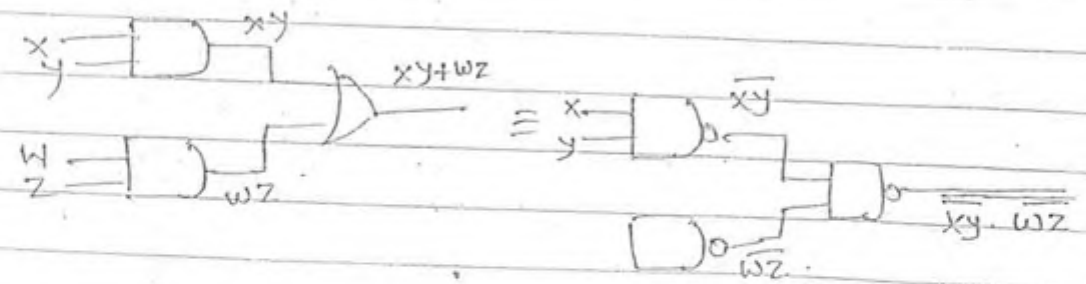
Sol:



Q. To implement $xy+wz$ minimum no. of two I/P Nand gate.

a)





Two level AND-OR = Two level NAND-NAND.

Q To implement $(A+B)(C+D)$ minimum number of NOR gate required

Sol: (3)

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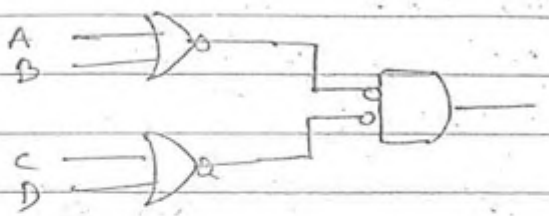


3

OR-AND $\Leftrightarrow$ NOR-NOR

POS → only NOR gates.

NB.

32 (a)

31 (b)

30 (c)

$AB + AC \; [(\overline{AB})(\overline{AC})]$

$\downarrow x \qquad \downarrow \bar{x}$

$= AB.$

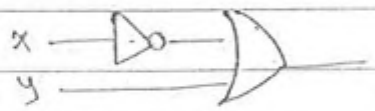
29 D

28 b

27 d

x	y	f
0	0	1
0	1	1
1	0	0
1	1	1

$\leftarrow \bar{x}+y$



24 (a)

23 Inverse function → Complement

$c \rightarrow a + bc \Rightarrow \bar{a}(\bar{b}+\bar{c})$

c - 1 a - 2

d - 4

$b \rightarrow (ab + \bar{a}\bar{b}) + c$

$(a \oplus b) \cdot c$

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21 (d) $A\bar{D} + ABCD + A\bar{C}D + \bar{A}B + \bar{A}\bar{B}$

$A\bar{D}(1 + C + BC) + \bar{A}(B + \bar{B})$

$\bar{A} + A\bar{D} = \bar{A} + D$

20 (A)

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

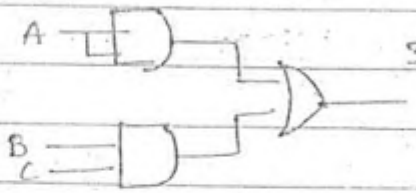
$\bar{A}BC + AB\bar{C}$

$B[\bar{A}C + A\bar{C}]$

$B[A + C][\bar{A} + \bar{C}]$

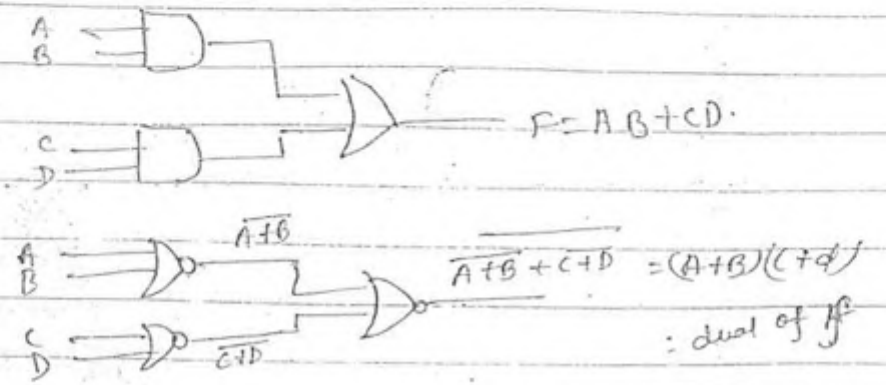
19 $A + BC$

$A \cdot A + BC$



18 a

17 (c)



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→ AND $\xleftrightarrow{\text{Dual}}$ OR

NAND $\xleftrightarrow{\text{Dual}}$ NOR

EXOR $\xleftrightarrow{\text{Dual}}$ EXNOR

NOT $\longleftrightarrow$ NOT

16

15 $X \oplus Y \rightarrow (4)$

14 (C)

13 (A)

12 $(\bar{A}+B)(\bar{A}+\bar{C})(\bar{B}+\bar{C})$

$= (\bar{C}+A\bar{B})(\bar{A}+B)$

$= \bar{A}\bar{C} + B\bar{C}$

$= \bar{C}(\bar{A}+B)$.

11 C D

10

9 D

8 A, C

7 (b)

6 (a)

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Digital circuit

Combinational Circuit	Sequential Circuit
→ Present o/p depends on only present i/p.	Present o/p → Present i/p, Previous present o/p.
→ No Feedback	Feedback
→ No Memory	Memory.
Ex H.A	Ex:- Flip-flop
F.A	Register
MUX	Counters.
DeMUX	

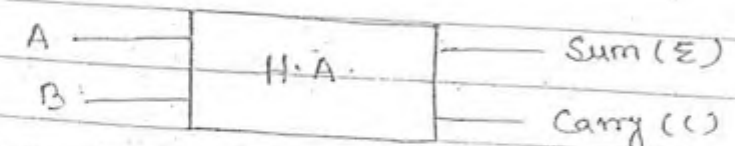
☆ Combinational Circuit :→

⇒ Procedure To Design Combinational Circuit :→

1) Identify inputs and outputs.
2) Construct truth table.
3) Write logical expression in SOP or POS.
4) Minimize logical expression.
5) Implement Logic circuit.

⇒ Arithmetic Circuit

1 Half Adder :→



Truth table:-

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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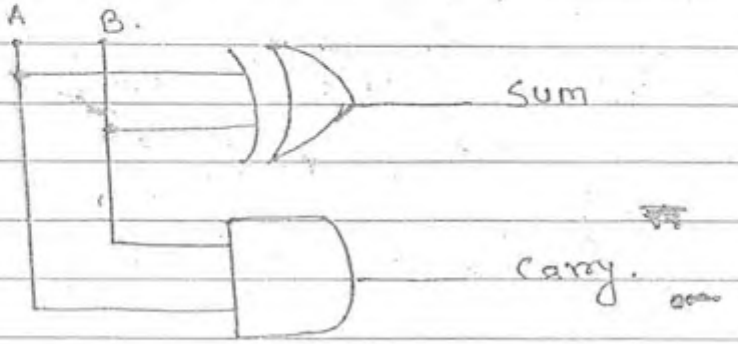
→ Logical Expression :-

Sum = $\bar{A}B + A\bar{B} = A \oplus B$

Carry = AB

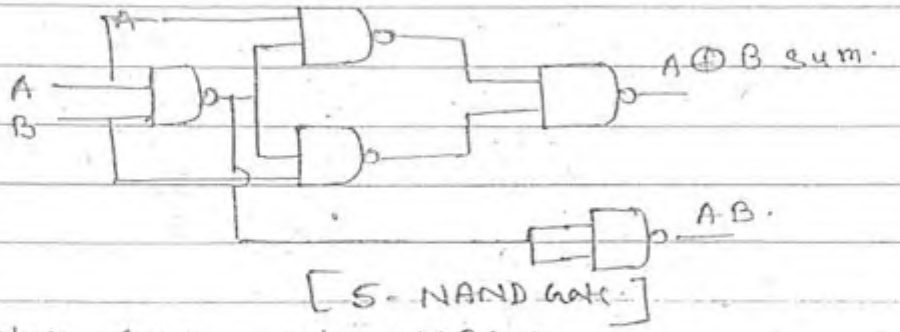
→ Implement :-



1) Logical Expression of SUM
2) Logical expression of Carry
3) Minimum no. of NAND. (5)
4) Minimum no of NOR (5)
5) No. of MUX
6) No. of Decoders.

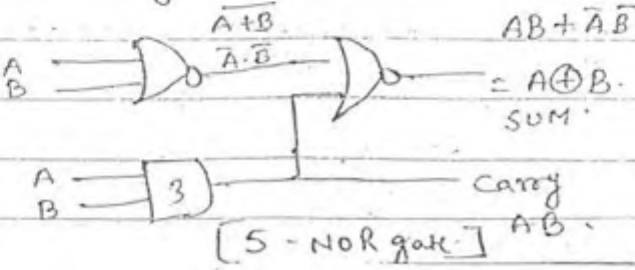
Q. Implement HA into NAND gate?

Sol: Half Adder Using NAND :-



[5 - NAND Gate]

Half Adder using NOR :→



[5 - NOR gate]

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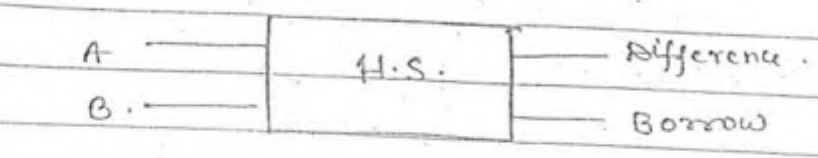
2. Half Subtractor :→



→ Truth table

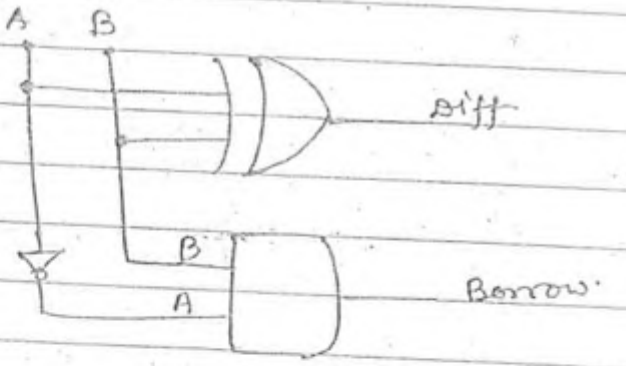
A	B	Diff (A-B)	Borrow.
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

→ Logical Expression :-

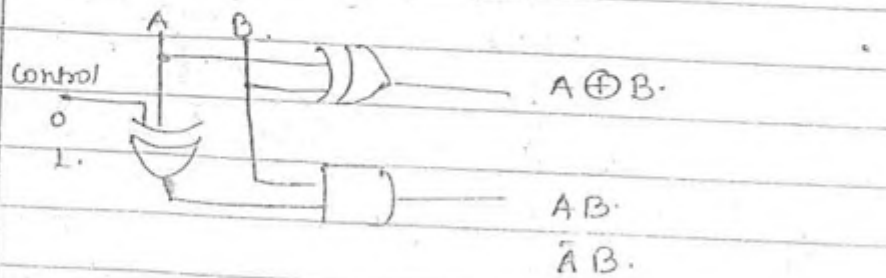
Difference = $\bar{A}B + A\bar{B} = A \oplus B$.

Borrow = $\bar{A}B$.

→ Implement :-



→



Control = 0 → Half Adder.

Control = 1 → Half Subtractor.

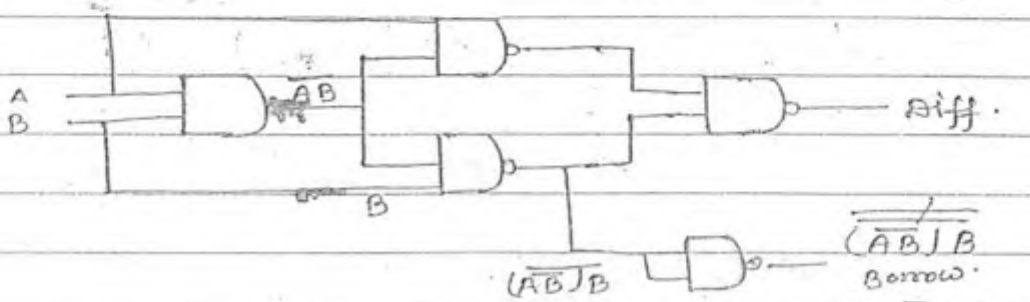
→ No. of NAND gate. (5)

→ No. of NOR gate (5)

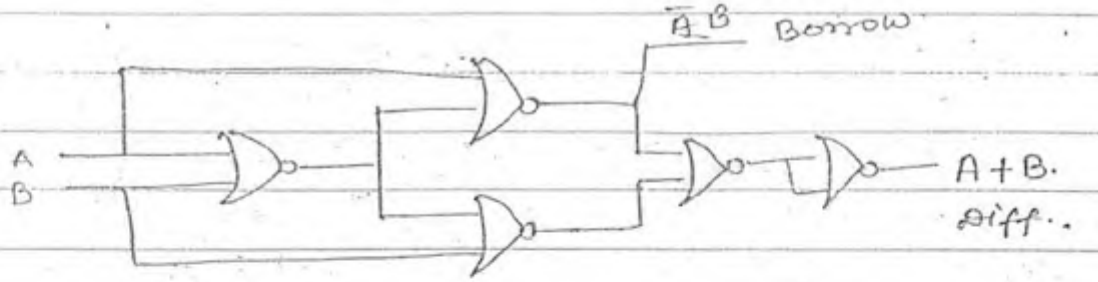
→ No. of MUX

→ No of Decoder.

→ Implementation of Half Substractor using NAND Gate :→

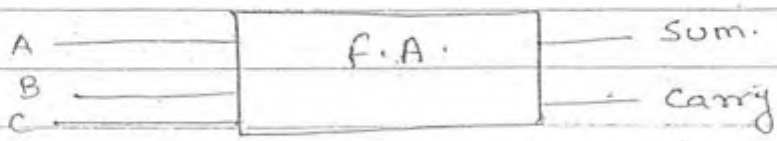


→ Implementation of Half Substractor using NOR gate :—



NOR - 5

3) Full Adder :—



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→ Truth table.

A	B	C	Sum.	Carry.
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1.
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1.
1	1	1	1	1

→ Logical Expression :→.

$SUM = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= A \oplus B \oplus C.$

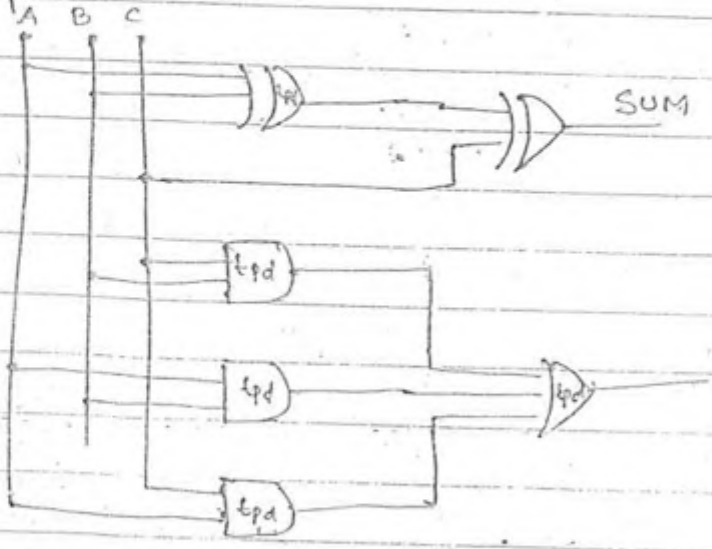
$= \Sigma m(1, 2, 4, 7)$

$Carry = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= AB + BC + AC$

$= \Sigma m\ (3, 5, 6)$

→ Implement :-



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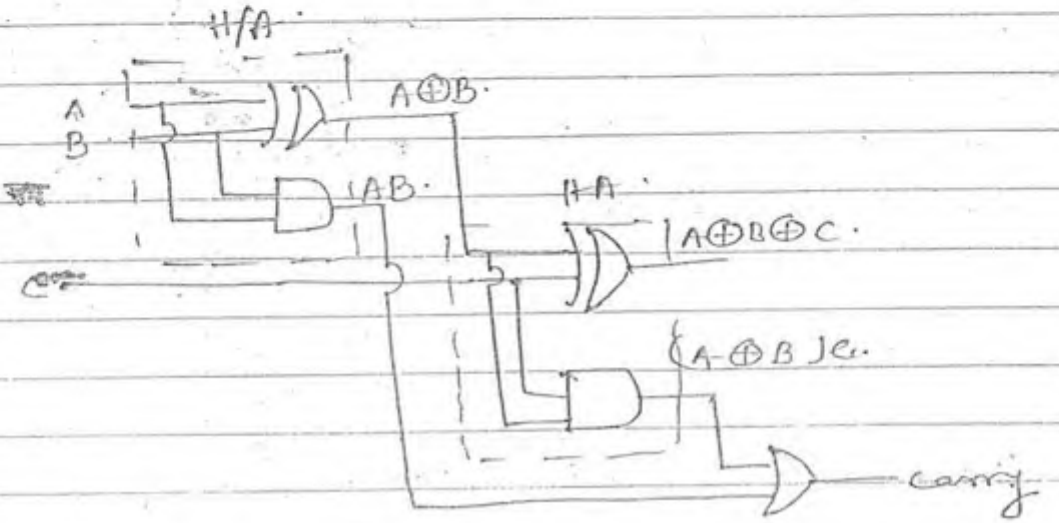
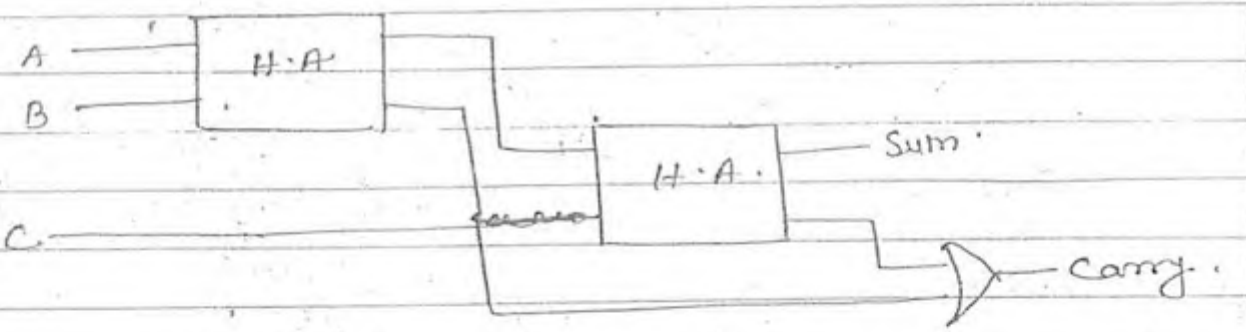
In full Adder each logic gate have propagation delay of t_{pd} to provide sum or carry O/P it require $2t_{pd}$.

$$\text{Carry} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC.$$
$$= AB + C(\bar{A}B + A\bar{B})$$





1) Logical exp Sum
2) Logical exp Carry
3) No. of HA & OR.
4) Minimum no. of NAND. (9)
5) Minimum no. of NOR. (7)
6) No. of MUX
7) No. of DeMUX

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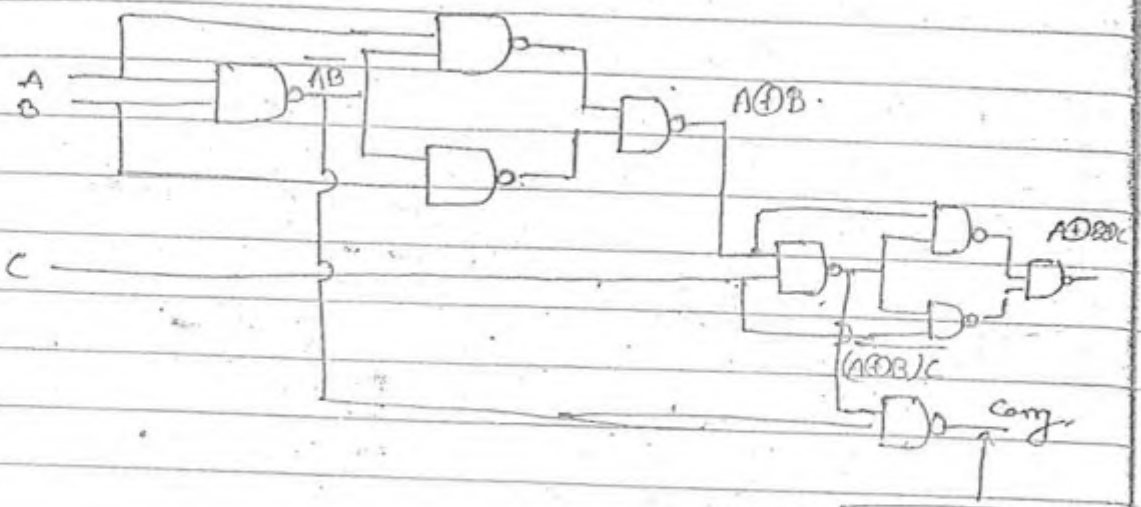
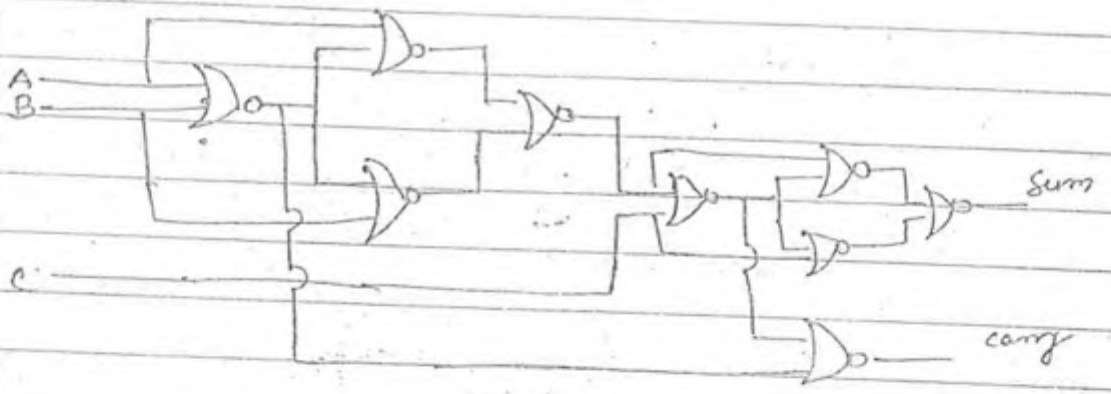
Implimentation of Full Adder Using NAND Gates :→



$(\overline{AB})(\overline{A \oplus B \oplus C})$

$AB + (A \oplus B)C.$

Implimentation of Full Adder Using NOR Gates :→



⇒ Parallel Adder :→

→ In Serial Adder only one Full Adder is used to add group of bit. It is slowest adder.

```
  1 1 0 1
  1 0 1 1
-------------
1 1 0 0 0
```

→ 4 bit → 3F·A or 1H·A

4F·A or

7H·A

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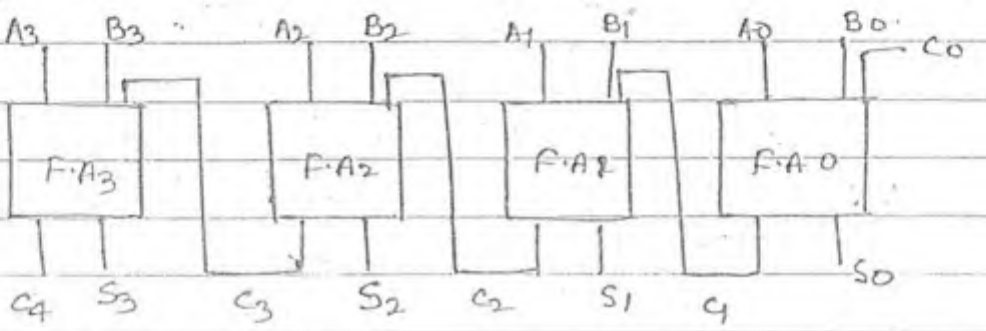
Parallel Adder is used to add group of bits:
To add two n-bit numbers it requires (n-1) Full Adder and one Half Adder or n Full Adder or (2n-1) HA & (n-1) OR gates.

→ 4 bit Parallel Adder :→ [Ripple carry Adder]

A_3 A_2 A_1 A_0
1 0 1 1
1 1 0 1
B_3 B_2 B_1 B_0



C_4 → Carry.
S_3 S_2 S_1 S_0 → Sum.

→ In parallel Adder propagation delay travel from I/P to o/p carry hence it is also known as Ripple carry Adder
→ In parallel Adder each full adder provide two logic gate delay.
→ In n-bit Parallel Adder to provide final result it required 2ntpd.

W.B 2011

1 add → 100ns.
1s → $\frac{1}{100 \times 10^{-9}} = 10^7$ add.

→ Disadvantages :→
→ Carry propagation delay will present as no of bit is increases speed of operation is reduced to avoid this

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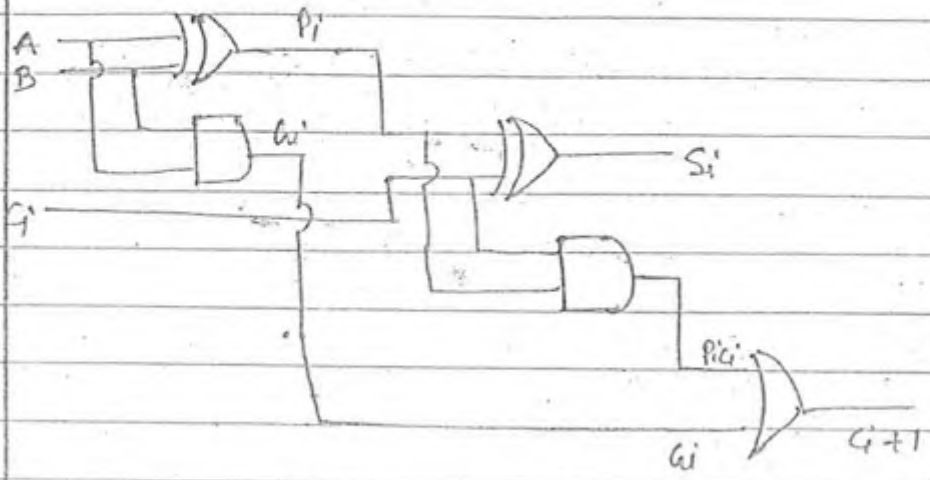
Look ahead carry adder is used.

→ Look Ahead Carry Adder:→



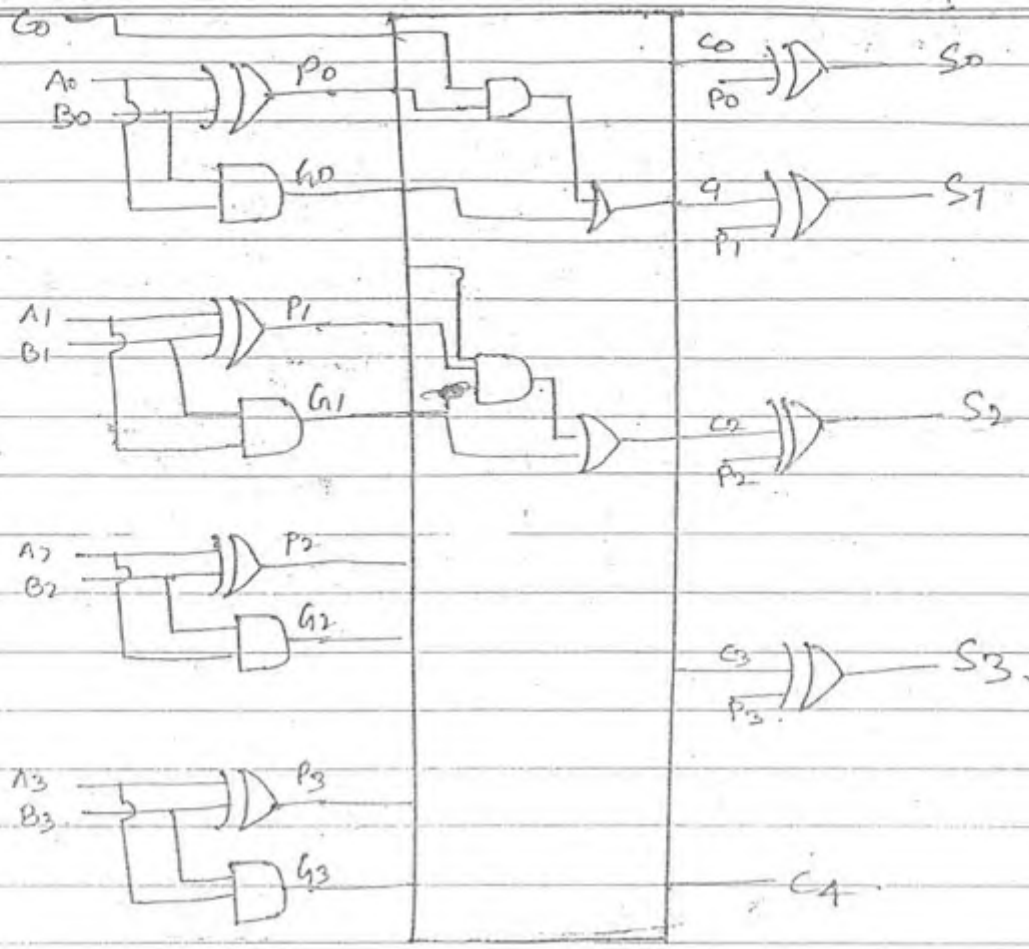
Where P_i = Propagation.
G_i = Generation term.

$P_i = A_i \oplus B_i$ $\quad A_3\ A_2\ A_1\ A_0$
$G_i = A_i B_i$ $\quad B_3\ B_2\ B_1\ B_0$
$S_i = P_i \oplus C_i$
$C_{i+1} = P_i C_i + G_i$ → Look ahead carry generation equation.

→ 4-bit Look Ahead Carry Adder:→

$P_0 = A_0 \oplus B_0$ $\quad G_0 = A_0 B_0$ $\quad S_0 = P_0 \oplus C_0$
$P_1 = A_1 \oplus B_1$ $\quad G_1 = A_1 B_1$ $\quad S_1 = P_1 \oplus C_1$
$P_2 = A_2 \oplus B_2$ $\quad G_2 = A_2 B_2$ $\quad S_2 = P_2 \oplus C_2$
$P_3 = A_3 \oplus B_3$ $\quad G_3 = A_3 B_3$ $\quad S_3 = P_3 \oplus C_3$

C_0 → Input Carry.
$C_1 = P_0 C_0 + G_0$
$C_2 = P_1 C_1 + G_1 = P_0 C_0 + P_1 G_0 + G_1$
$C_3 = P_2 C_2 + G_2 = P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2$
$C_4 = P_3 C_3 + G_3$
$= P_3 P_2 P_1 P_0 C_0 + P_3 P_2 P_1 P_0 G_0 + P_3 P_2 G_1 + P_3 G_2 + G_3$



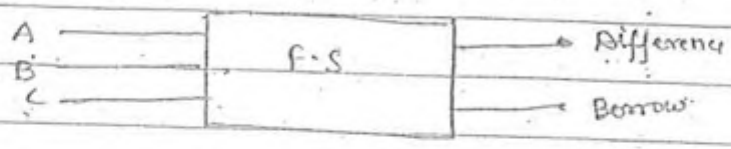
In look ahead carry adder to provide carry o/p it require three logic gates.
To provide Sum o/p it require 4 logic gates.
Carry ckt is implimented with two level AND-OR gate.
No. of AND gate required in carry ckt = $n\frac{(n+1)}{2}$

No of OR gate required in carry ckt = n.

5) c Duty cycle = $\frac{t_{ON}}{t} \times 100$

$= \frac{1.7 - 0.4}{2.2 - 0.4} \times 100 = 72\%$

☆ Full Subtractor :-



→ Truth table :-

A	B	C	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

→ Logic Expression

Difference :- $A \oplus B \oplus C$

Borrow = $\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$

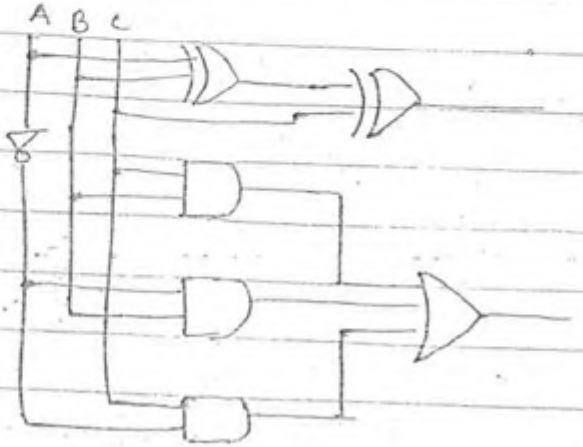
$= \bar{A}B(C+\bar{C}) + \bar{A}C(B+\bar{B}) + BC(A+\bar{A})$

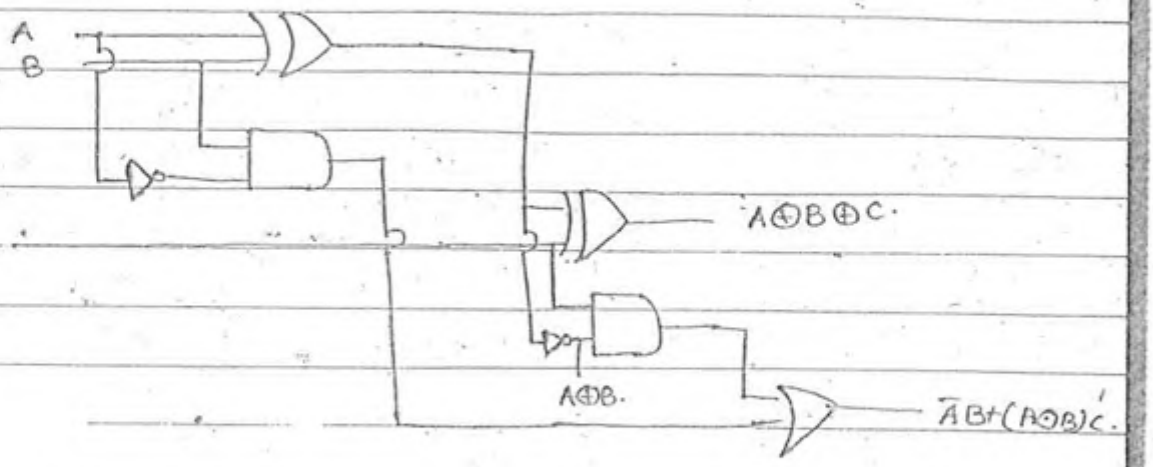
$= \bar{A}B + \bar{A}C + BC$

$= \sum m(1,2,3,7)$

$= \bar{A}B[C+\bar{C}] + [\bar{A}\bar{B}+AB]C$

→ Implement :- $\bar{A}B + (A \oplus B)C$



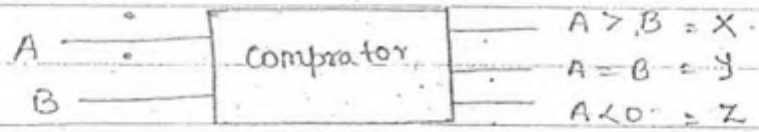


F.S → 2 H.S and 1 O R.

NAND - 9

NOR → 9.

✡ Comprator :→



→ Truth table :-

A	B	X (A>B)	Y (A=B)	Z (A<B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

→ Logic Expression :→

$X = A\bar{B}$

$Y = \bar{A}\bar{B} + AB$

$Z = \bar{A}B$

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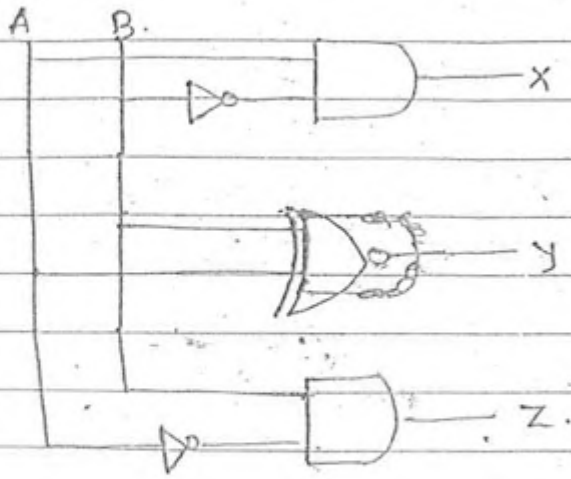
Implement :→



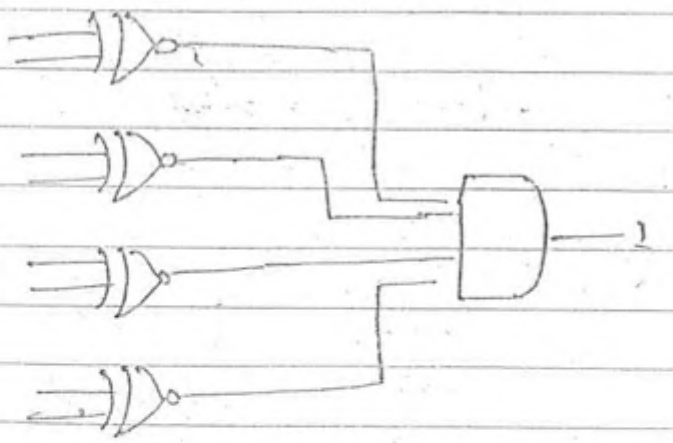
☆ 4 bit Comprator :→

$A_3\ A_2\ A_1\ A_0 \longrightarrow A$

$B_3\ A_2\ B_1\ B_0 \longrightarrow B.$

4	3	5	2
4	3	5	2

$(A_3 \odot B_3) \cdot (A_2 \odot B_2) \cdot (A_1 \odot B_1) \cdot (A_0 \odot B_0)$



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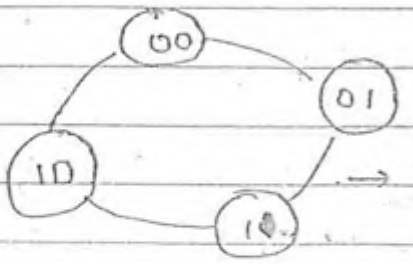
K-Map :→



→ Differ by 1 bit.

In K-map gray code representation is used.

→ 2 Variable K-map :-

A \ B	0	1
0	0 00	1 01
1	2 10	3 11

→ 3-Variable K-map :→

A \ BC	00	01	11	10
0	0	1	3	2
1	4	5	7	6

→ Four-variable K-map :-

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

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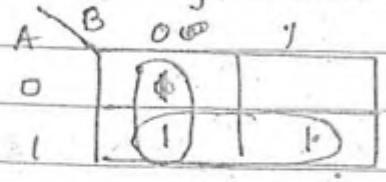
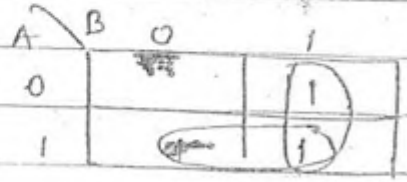
→ SOP :—

$f(A,B) = \sum m(0,2,3)$



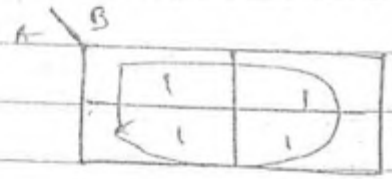
A + B.

Q. $f(A,B) = \sum m(1,2,3)$



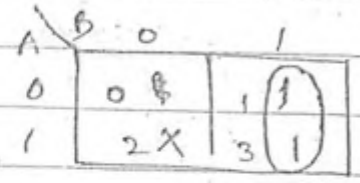
A + B.

Q $f(A,B) = \sum m(0,1,2,3)$.

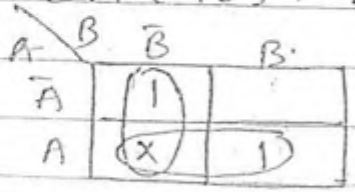


1.

Q $f(A,B) = \sum(1,3) + \sum d(2)$

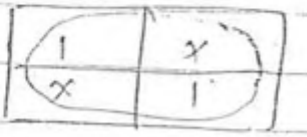


Q. $f(A,B) = \sum m(0,3) + \sum d(2)$



A + B̄

Q $f(A,B) =$



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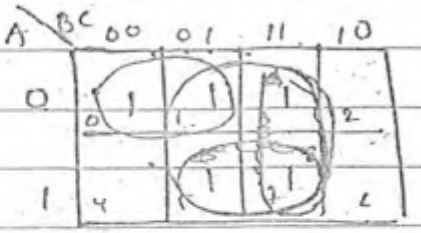
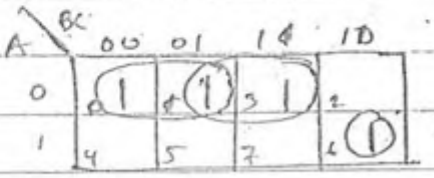
Q $f(A,B,C) = \Sigma m(0,1,3,5,7)$



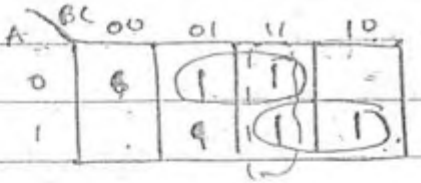
$C + \bar{A}\bar{B}$

Q $f(A,B,C) = \Sigma m(0,1,3,6)$



$\bar{A}\bar{B} + \bar{A}C + AB\bar{C}$

Q. $f(A,BC) = \Sigma m(1,3,6,7)$

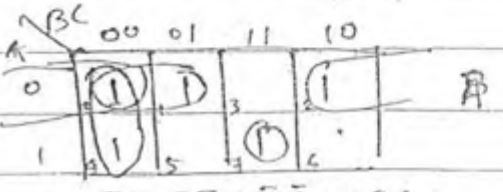


$\bar{A}B + AB + B\bar{C}$ → Redundent.
×

☆ Procedure to Draw K-map:-

1) Octets
2) Squads
3) ~~Parts~~ Pairs
4) Single term.
5) Remove redundent

Q $f(A,B,C) = \Sigma m(1,2,4,7)$



$\bar{A}B + B\bar{C} + \bar{A}\bar{C} + ABC$.

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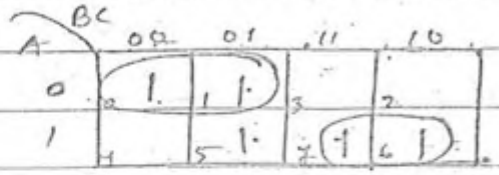
Q. $f(A,B,C) = \Sigma m(0,1,5,6,7)$



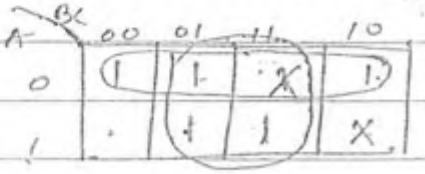
$A\bar{B} + \bar{A}\bar{B} + AC$

$A\bar{B} + \bar{A}\bar{B} + \bar{A}C$

NOTE:

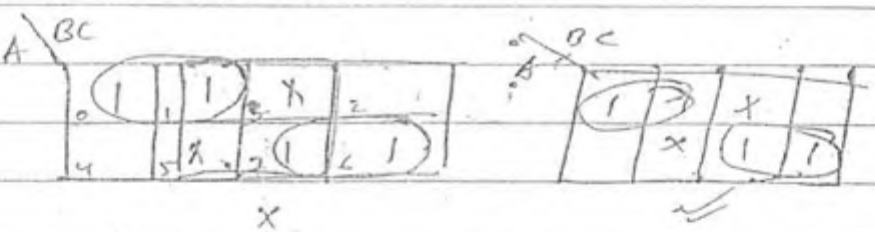
→ K-map provides minimize expression but not necessarily unique

Q $f(A,B,C) = \Sigma m(0,1,2,5,7) + \Sigma d(3,6)$



$\bar{A} + C$

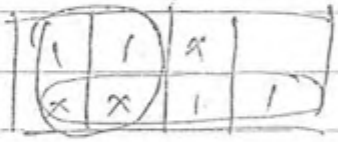
Q $f(A,B,C) = \Sigma m(0,1,6,7) + \Sigma d(3,5)$



$\bar{A}\bar{B} + AB$

Q. $f(A,B,C) = \Sigma m(0,1,6,7) + \Sigma d(3,4,5)$

$A + \bar{B}$



Q $f(A,B,C,D) = \Sigma m(0,1,3,5,7,8,9,11,13,15)$

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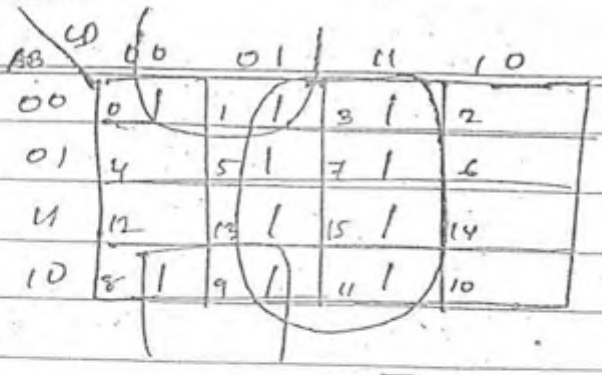
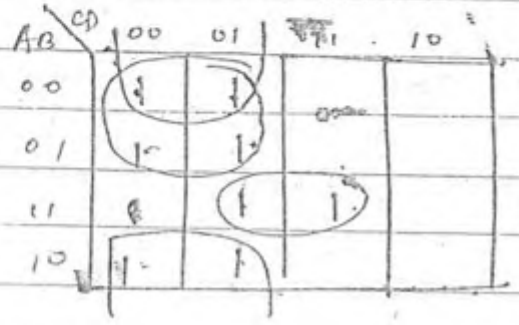


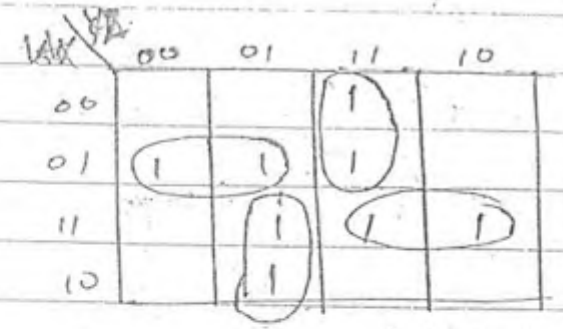
$D + \bar{B}\bar{C}$

Q. $f(A,B,C,D) = \sum m(0,1,4,5,8,9,13,15)$



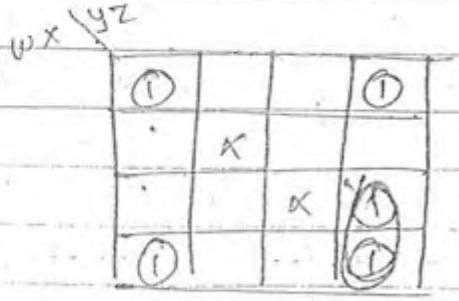
$\bar{A}\bar{C} + \bar{B}\bar{C} + ABD$

Q.



4-pair → (B) one

Q.



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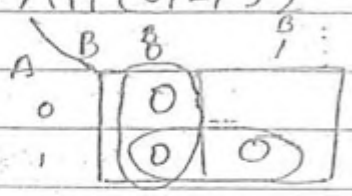
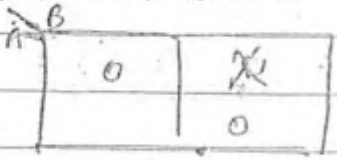
→ POS :-

Q $f(A,B) = \pi M(0,2,3)$



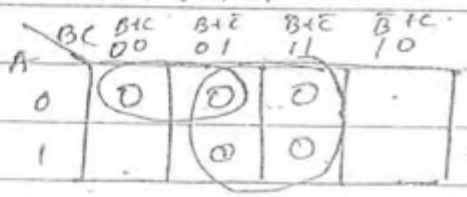
$\bar{A} \cdot B$

Q $f(A,B) = \pi M(0,3) + \pi d(1)$



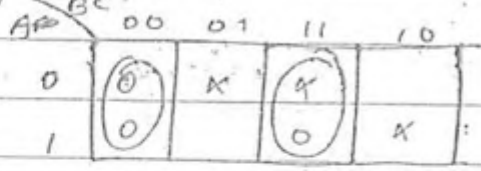
$A \cdot \bar{B}$

Q $f(A,B,C) = \pi M(0,1,3,5,7)$



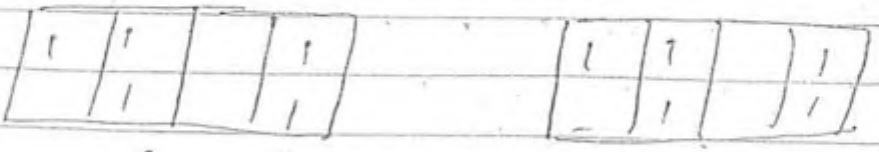
$\bar{C} \cdot (A+B)$

Q for the given K-map minimised POS expression.



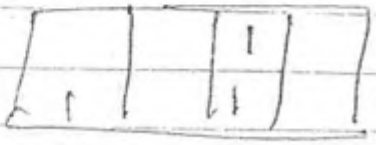
$(B+C)(\bar{B}+\bar{C})$

Q



x y

$x = y$



$z = \bar{x}$

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PQ \ RS	$\bar{R}\bar{S}$	$\bar{R}S$	RS	$R\bar{S}$	
$\bar{P}\bar{Q}$		1	1	1	1
$\bar{P}Q$	1	1	1	1	ϕ
PQ		1	1	1	1
$P\bar{Q}$		1	1	1	1

M

X

	1	1	1
1	1	1	1
	1	1	1
	1	1	1

Z

M = Z

M = $\bar{X}$

Z = $\bar{X}$

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	6

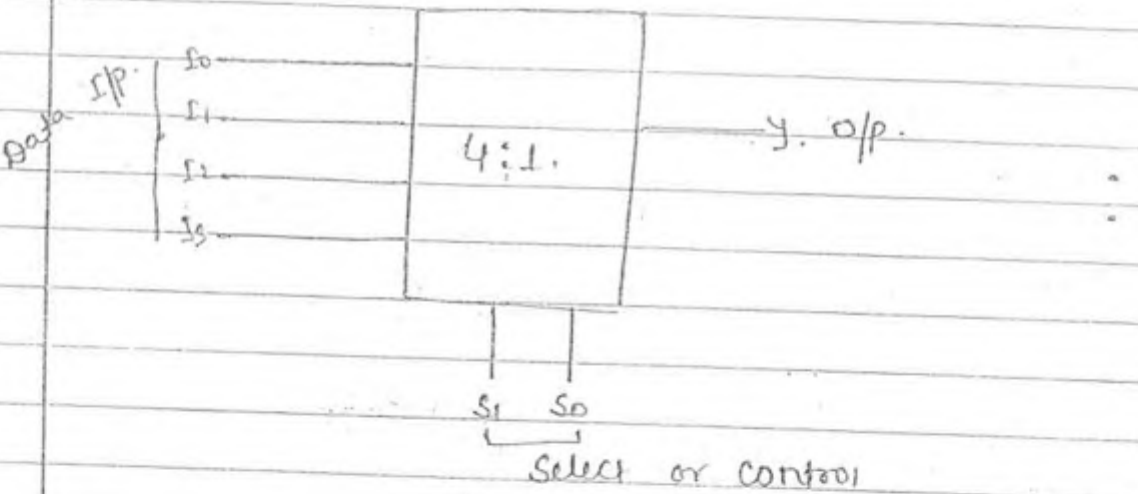
$Y = \bar{A}\bar{B}\cdot 0 + \bar{A}B\cdot 1 + A\bar{B}\cdot 0 + AB\cdot 6$

$= \bar{A}B + ABC$

$= B(\bar{A} + AC)$

$= B(\bar{A} + C)$

☆ Multiplexer :→



It is a combinational ckt which have many data I/P and single o/p depending on control or select I/P one of the I/P transfer to the o/p.

→ Control or Select :→

1) Data Selector
2) Many to one ckt
3) Universal logic ckt
4) Parallel to Serial

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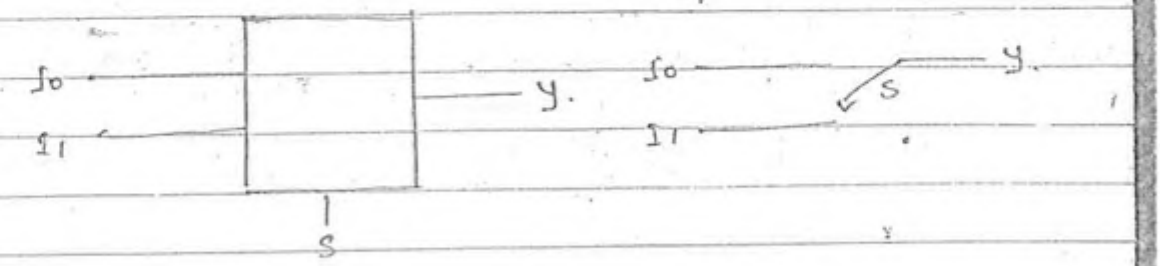
$m = 2^n$

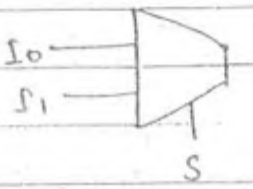
$n = \log_2 M$ Where,

M = no. of data I/P

n = Select I/P

⇒ 2 : 1 Multiplexer :→

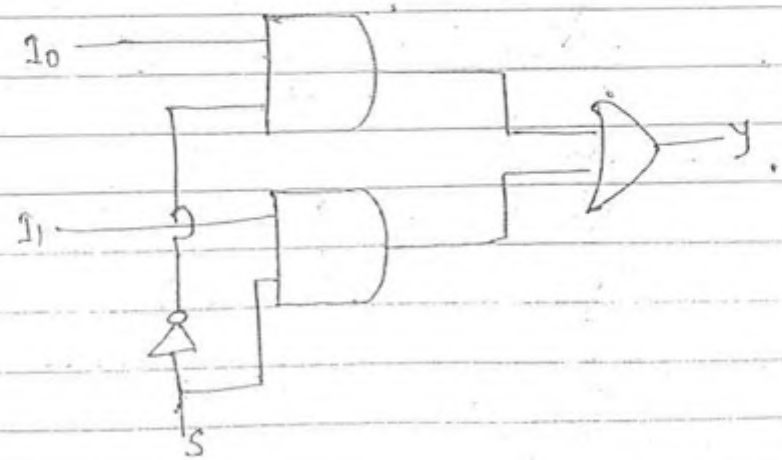




→ Truth table.

S	Y.
0	I_0
1	I_1

$$Y = \bar{S} I_0 + S I_1$$



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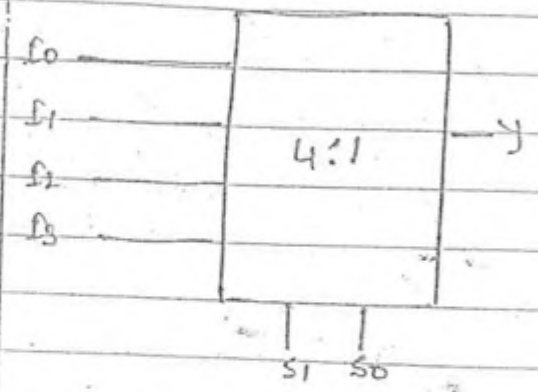
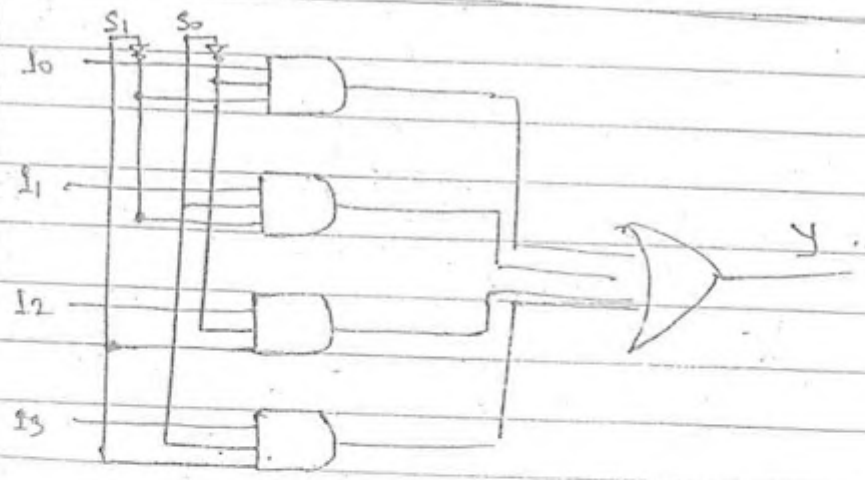
⇒ 4:1 Multiplexer :→



→ Truth table :—

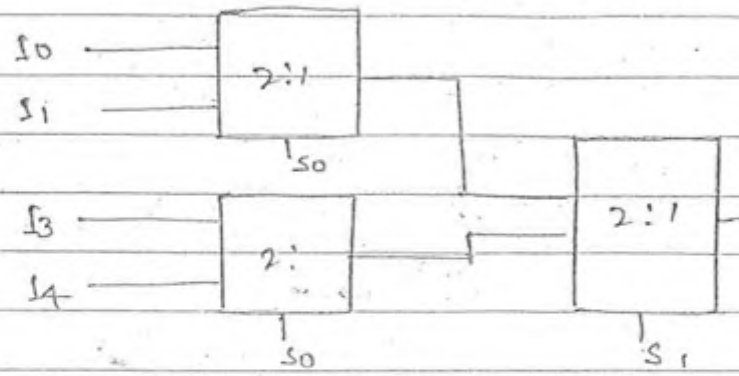
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$



⇒ Implimentation of Higher order MUX With Lower order :—

1) 4 x 1 ⟶ (3) ⟶ 2 x 1



2) ~~Implement~~ 8 × 1 ——— 2 × 1

4 + 2 + 1 = 7

3) 16 × 1 ——— 2 × 1

8 + 4 + 2 + 1 = 15

4) 64 × 1 ——— 2 × 1

63

5) 256 × 1 ——— 2 × 1

255

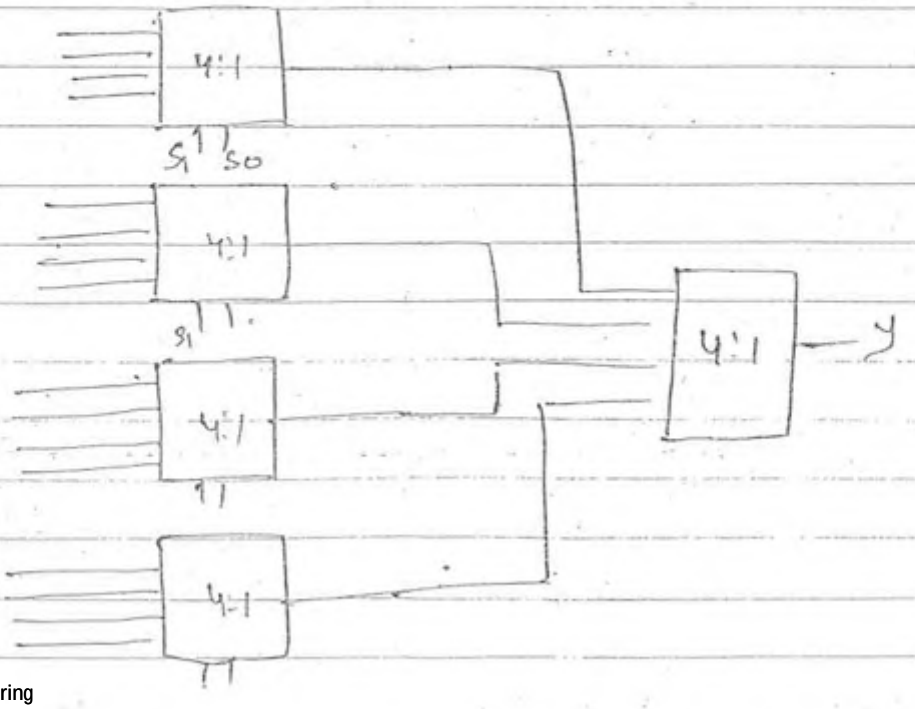
2^n × 1 ——— 2 × 1

$2^n - 1$

6) 16 × 1 ——— 4 × 1

4 + 1 = 5

7)



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7. 64x1 ——— 4x1

16+4+1 = 21

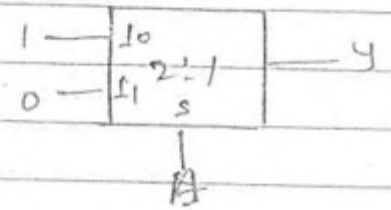
8) 64x1 ——— 8x1

8+1 = 9

9) 256x1 ——— 16x1

16+1 = 17.

⇒ Multiplixer As Universal :→



$Y = \bar{S} y_0 + S I_1$

$= \bar{A} \cdot 1 + A \cdot 0$

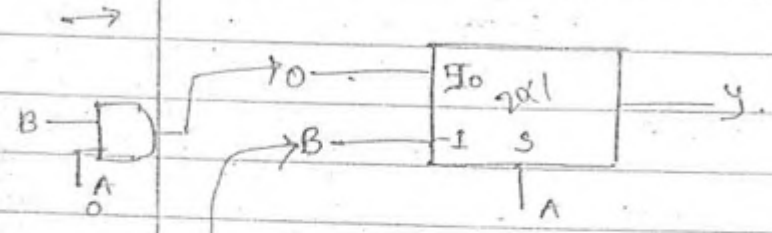
$= \bar{A}$ 1 NOT gate required

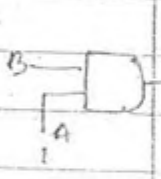
A Y

0 → 1

1 → 0

→



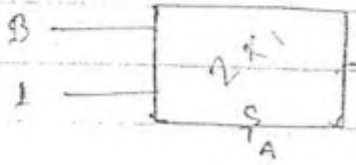


$Y = \bar{S} I_0 + S I_1$

$= \bar{A} 0 + A \cdot B$

$= AB.$

Q. Implement OR using 2:1 Mux.



$Y = \bar{S} I_0 + S I_1$

$= \bar{A} B + A 1$

$= A + B.$

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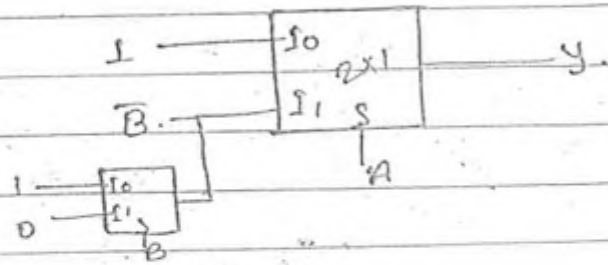
Q) Implement NAND gate using 2×1 Mux.



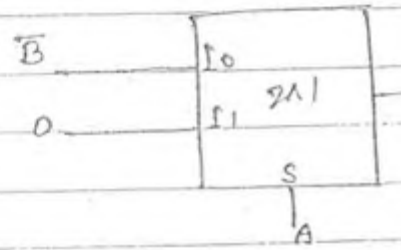
$Y = \bar{S} I_0 + S I_1$

$= \bar{A} \cdot 1 + A \bar{B}$

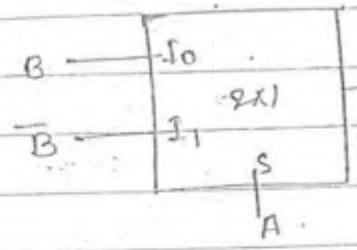
$= \bar{A} + \bar{B}$

$= \overline{AB}$

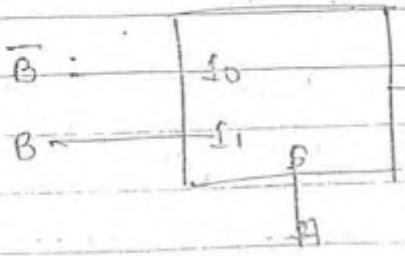
NOR :-



EXOR :-



EXNOR :-



Note :-

NOT, AND, OR → Require → 1 → 2×1 Mux.

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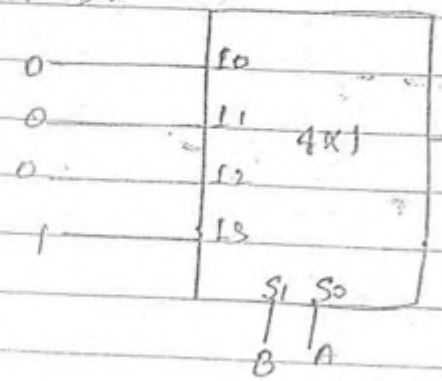
H·A — 3· — 2×1

H·S — 3 — 2×1

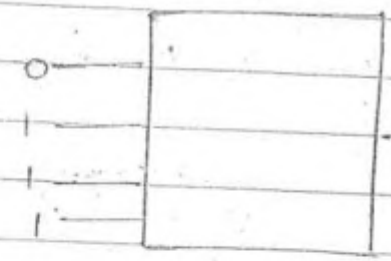
⇒ 4:1 MUX :—

→ AND :—



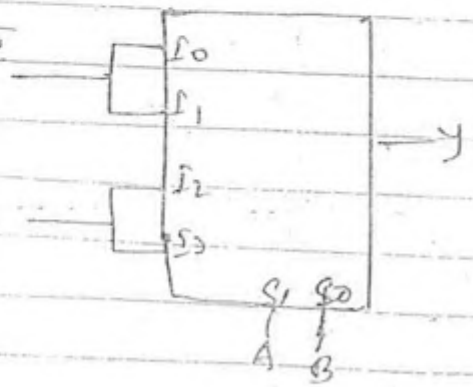
A	B·	y
0	0	0
0	1	0
1	0	0
1	1	1

→ OR :—



⇒ Determine minimised Logical Expression :—

Q. For the given 4×1 Mux minimised logical expression is



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$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$.

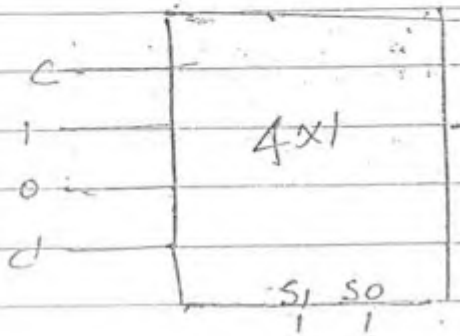
$= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$.

$= \bar{A}\bar{C}(B+\bar{B}) + AC(B+\bar{B})$

$= \bar{A}\bar{C} + AC$

$= A \odot C$.

Q.



$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$.

$= \bar{A}\bar{B}C + \bar{A}\cdot B\cdot 1 + A\bar{B}0 + AB\bar{C}$

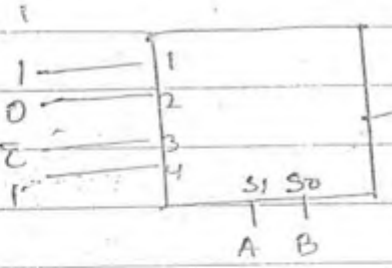
$= \bar{A}\bar{B}C + \bar{A}\cdot B(C+\bar{C}) + AB\bar{C}$

$= \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + AB\bar{C}$

$= \bar{A}C + B\bar{C}$ Ans

⇒ Implementation of Given Logical Expression :→

Q. Implement, $f(A,B) = \Sigma m(0,1,4,6,7)$ using 4x1 shown in fig.



Sol:	A	B	C			I_0	I_1	I_2	I_3
0	0	0	0 → $\bar{C}$	1	$\bar{C}$	(0)	2	(4)	(6)
1	0	0	1 → C.			(1)	3	5	(7)
2	0	1	0 → $\bar{C}$		C	1	$\bar{0}$	$\bar{C}$	1
3	0	1	1 → C.						
4	1	0	0 → $\bar{C}$						
5	1	0	1 → C.						
6	1	1	0 → $\bar{C}$	1					
7	1	1	1 → C						

4:1 MUX → 1

NOT → 1

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Q. Implement a logic expression.

$f(A,B,C) = \Sigma m(1,2,3,5,6,7)$

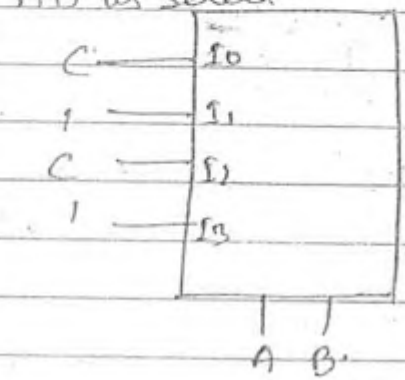
i) AB as select

ii) AC as select

iii) BC as select

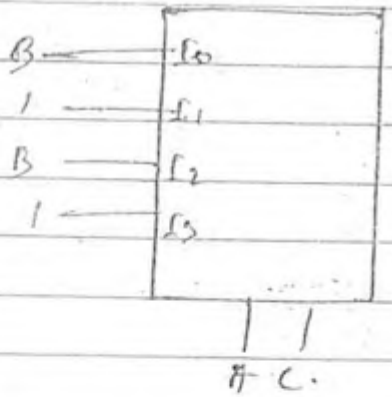
Sol:

i) AB as select



	I_0	I_1	I_2	I_3
$\bar{C}$	0	(2)	4	(6)
C	(1)	(3)	(5)	(7)
	$\bar{C}$	1	C	1

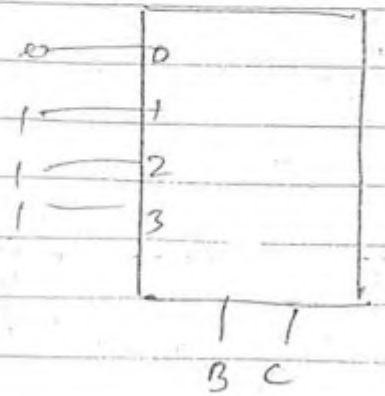
ii) AC as select



	I_0	I_1	I_2	I_3
$\bar{B}$	0	(1)	4	(5)
B	(0)	(3)	(6)	(7)
	B	1	B	1

$\bar{A}$	0	0	$\bar{B}$
$\bar{A}$	0	1	$\bar{B}$
$\bar{A}$	0	1	B
$\bar{A}$	0	1	B
A	1	0	$\bar{B}$
A	1	0	$\bar{B}$
A	1	1	B
A	1	1	B

iii) BC as select :-



S_0	I_1	I_2	I_3
0	(1)	(2)	(3)
4	(4)	(6)	(7)
0	1	1	1

using one 4x1 Mux any two variable function, some of three variable function can be implemented.
using one 4x1 Mux & one NOT all two variable function, all three variable function can be implement.

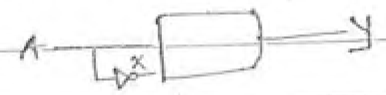
One 4x1 & one NOT → All two / All Three.

One 8x1 → All Three / Some four

One 8x1 & one NOT → All Three / All four

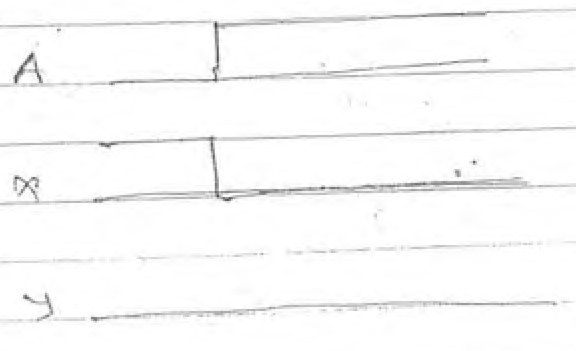
Q ~~Σm(0,1,4,...)~~

☆ Hazards :→



$Y = A \cdot \bar{A} = 0$.

Case I: for the given ckt determine O/P waveform when there is no propagation delay.



Static '0'

Case II
Determine O/P waveform for the given fig if there is a propagation delay of 1ns in NOT gate & no propagation delay in AND.

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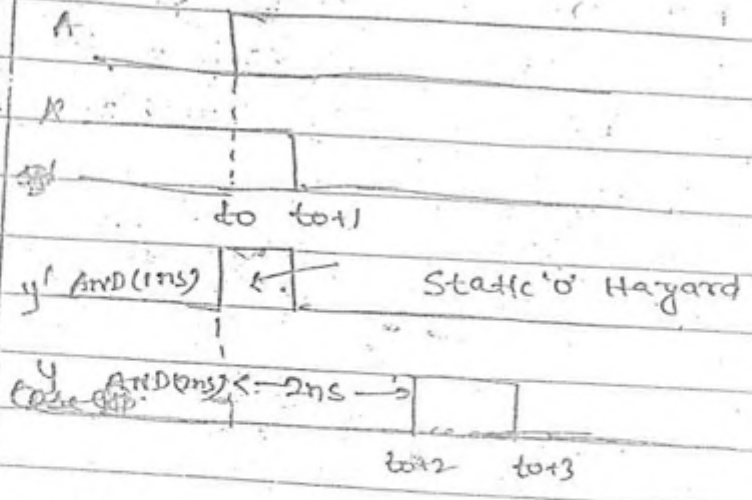
Sol:



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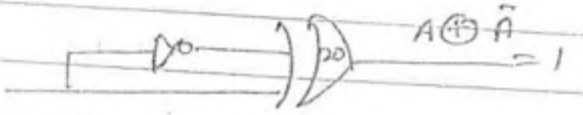
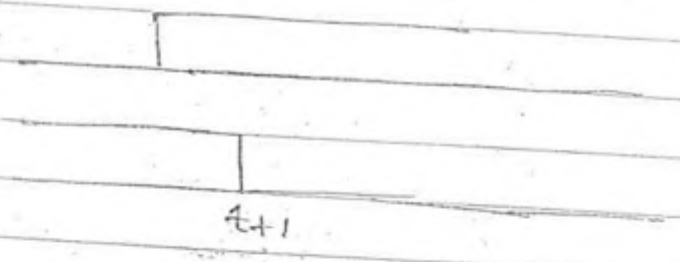
$t_1 = t_0 + 10ns$.

$t_2 = t_0 + 20ns$

$t_3 = t_0 + 30ns$.





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1) Hazards are unwanted change in the O/P due to propation delay.

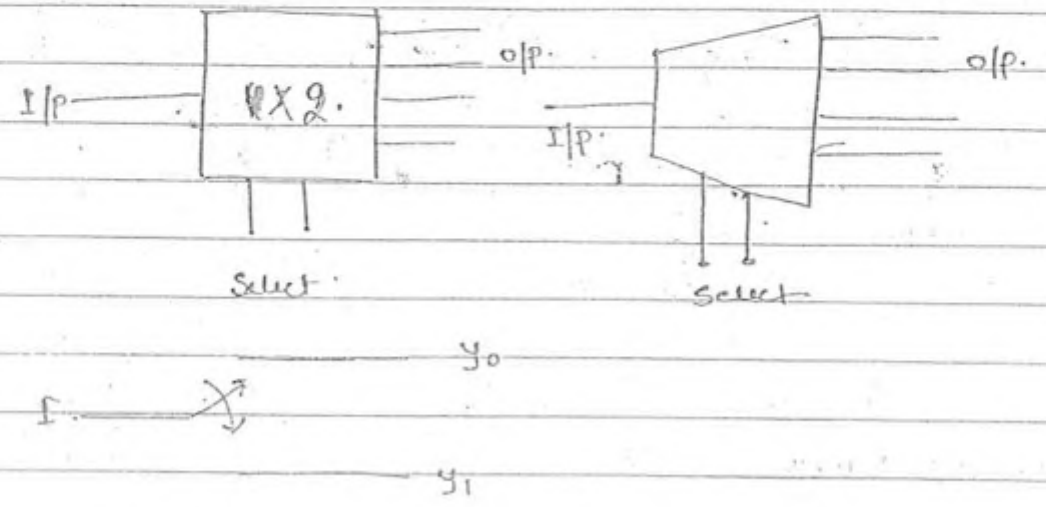
Hazard

- Static
  - occurs 2-Level Combinational ckt
    - Static '1' Two Level AND-OR
    - Static '0' Two Level OR-AND
- Dynamic Multilevel
- Essential. Asynchronous Sequential ckt.

To avoid static and dynamic hazard, redundent terms are added in the combinational ckt.

☆ DeMux :→

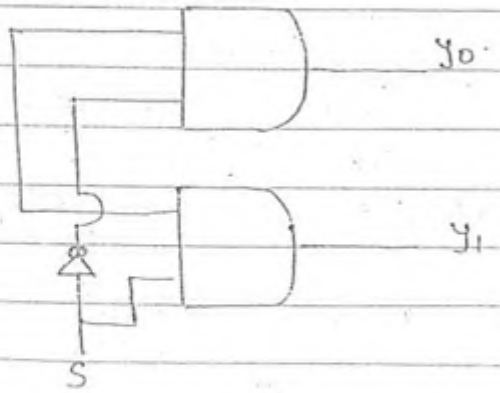
Demux is a combinational ckt which have one I/P and many (2^n) O/P depends upon selector I/P & control I/P is transfered to one of the many ckt.



→ Truth table :→

S	y_1	y_0
0	0	I
1	I	0

→ Implement :-



We cannot use DeMux as universal ckt.

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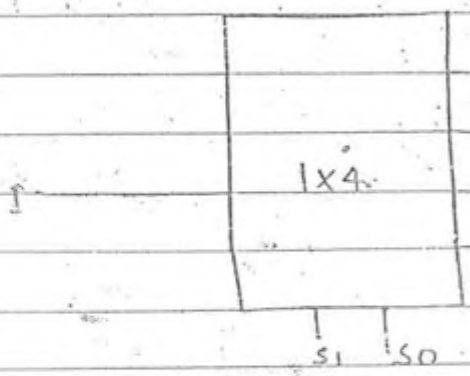
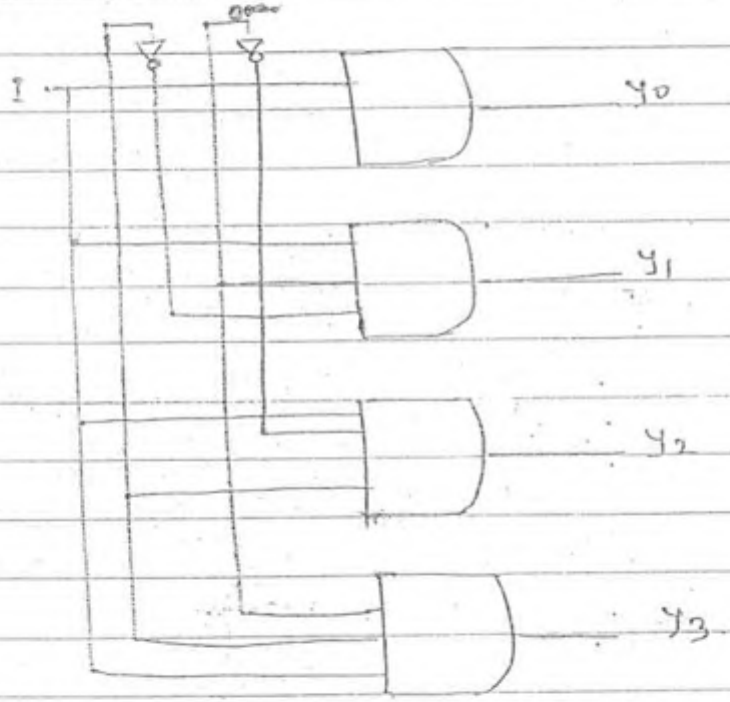
→ 1 : 4 Demux :→



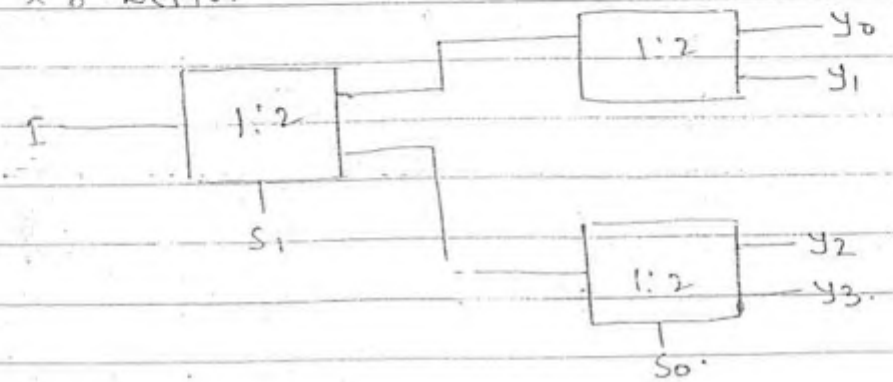
→ Implementation :-



→ 1 X 4 DeMUX — 3 — 1X2

4 X 1 MUX — 3 — 2 X 1

1 X 8 DeMUX — 7 — 1 X 2



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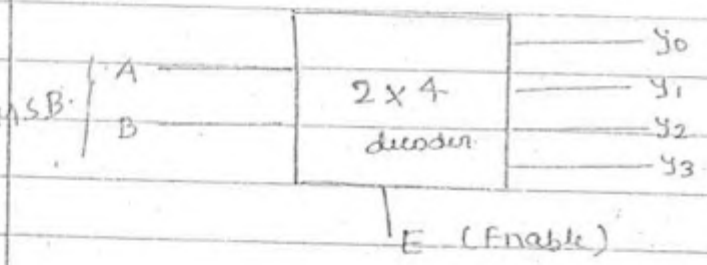
Decoder :→

→ Decoder is a combinational circuit which have many I/P and many o/p.

→ It is used to convert binary data into other code
- Binary to octal
- BCD to Decimal
- Binary to Hexa
- BCD to Seven segment.

Minimum Possible Decoder:-



→ Truth table:-

E	A	B	y_3	y_2	y_1	y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

$y_0 = \bar{A}\bar{B}E$

$y_1 = \bar{A}BE$

$y_2 = A\bar{B}E$

$y_3 = ABE$

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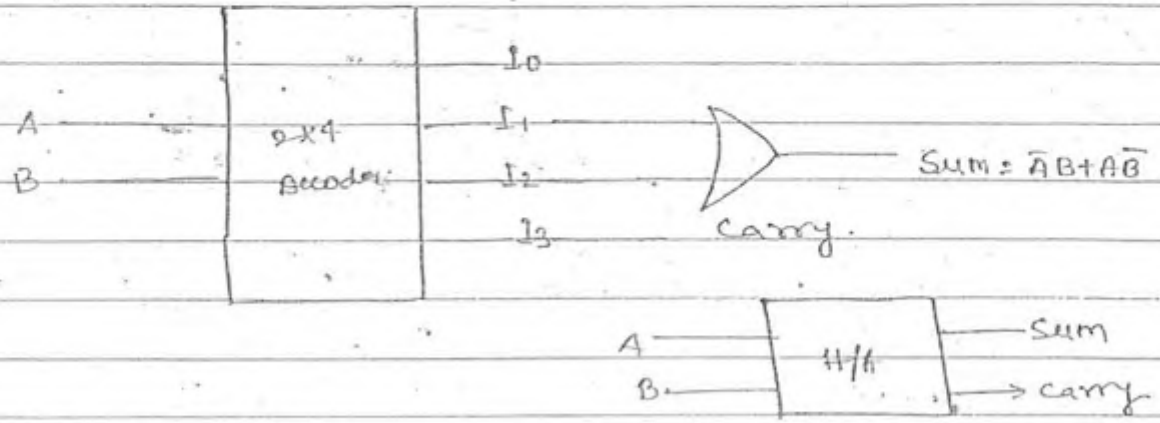
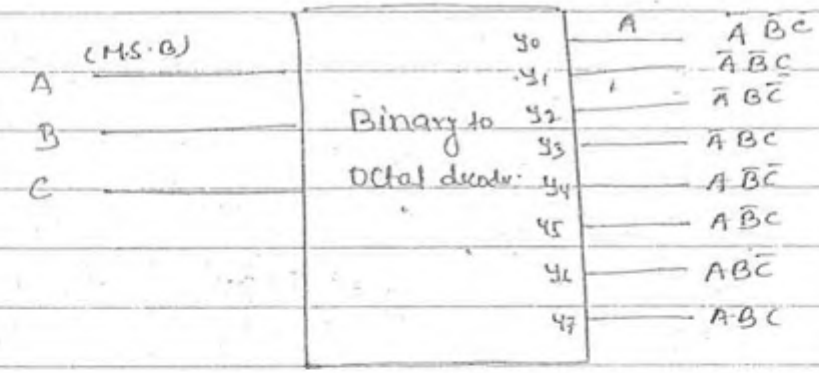
→ Decoder and Demux internal ckt remains same

Q Implement HA using 2×4 decoder.

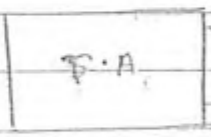
Sol:

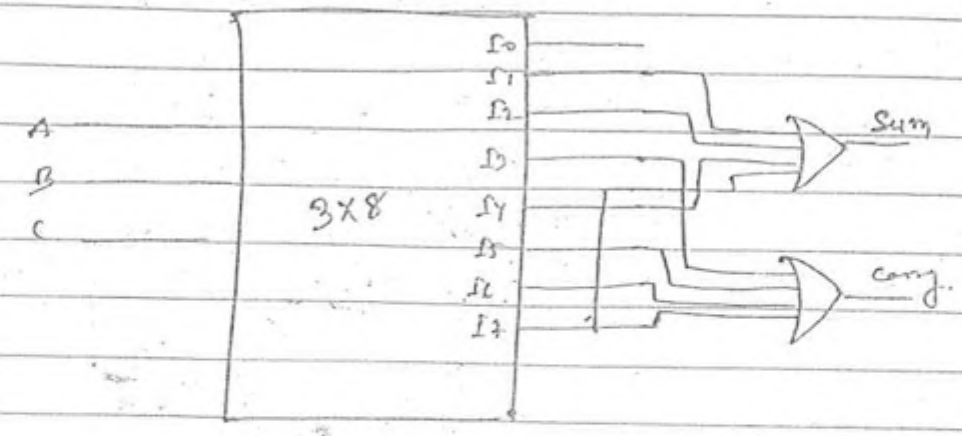


→ 3×8 Decoder (Binary to Octal Decoder) :-



→ Implement Full Adder :-



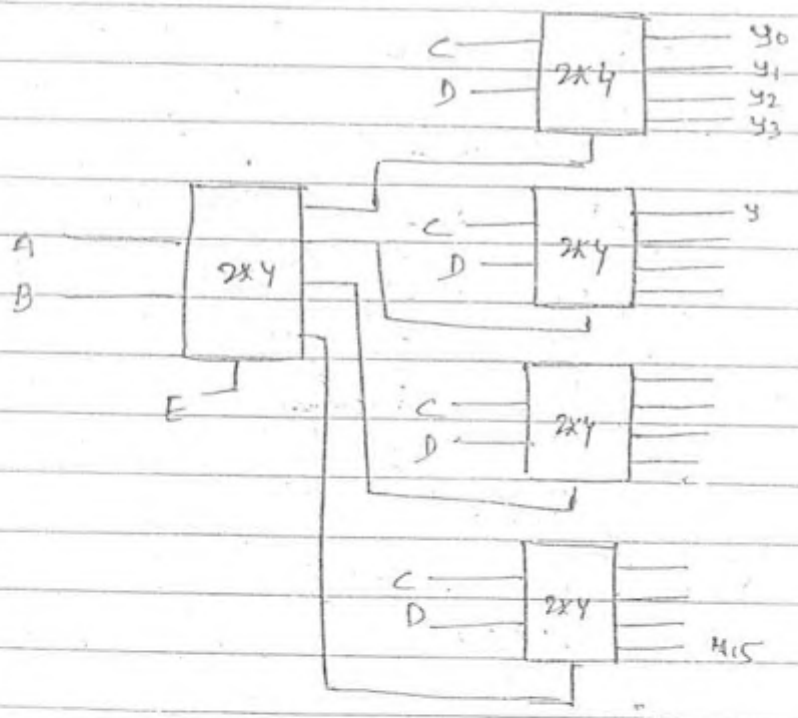


→ Implementation of higher order to lower order :→

4 x 16 ——— 5 ——— 2 x 4

1 x 16 Demux ——— 5 ——— 1 x 4 Demux

16 x 1 ——— 5 ——— 4 x 1



~~To implement~~

6 x 64 ——— 21 ——— 2 x 4

1+4+16

8 x 256 ——— 4 x 16.

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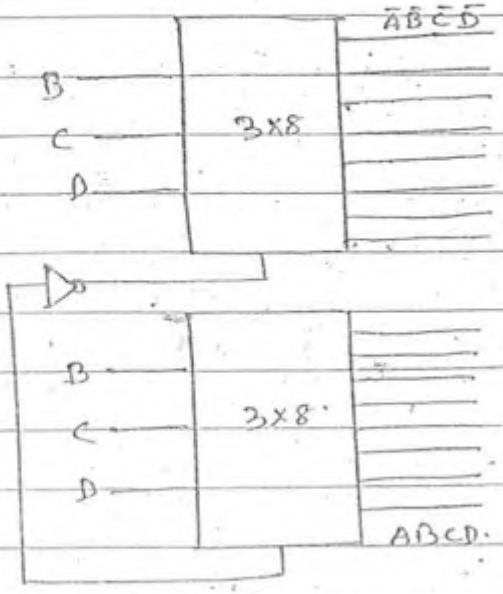
→ Implument 4x16 Decodir using 3:8 decoder :→



[2, 3x8 decoder, 1 NOT]

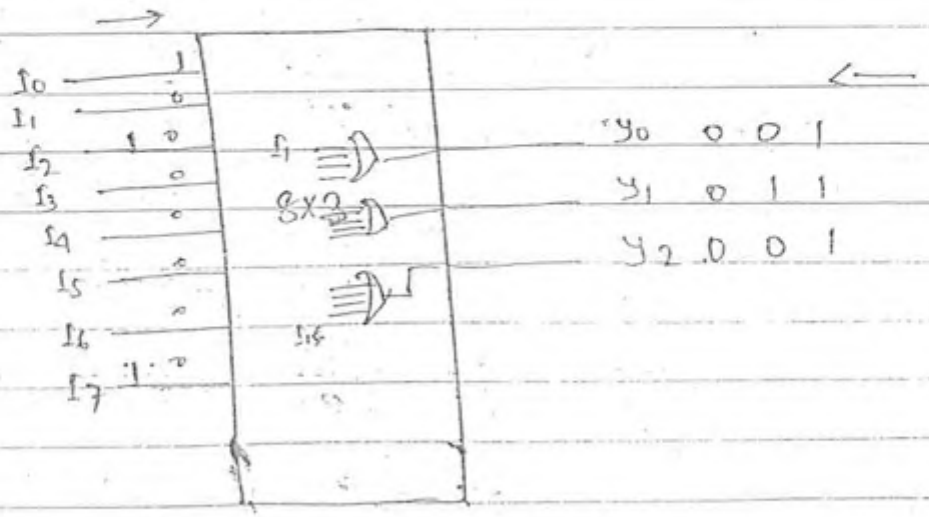
Encoder :→

→ It is combinational ckt which have many I/P & many o/P.

→ It is used to convert other codes to binary

* Octal to binary conversion
* Decimal to BCD
* Hex to Binary.

1 Octal to Binary Encoder.



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→ In normal encoder one of I/P is high and corresponding O/P is available at O/P.

→ In periority encoder, no. of I/P is high only highest periority corresponding binary is available at O/P.

→ Truth table :-

I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	Y_2	Y_1	Y_0	
0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	1	0	0	0	1	1
0	0	0	0	0	1	0	0	0	1	0	2
0	0	0	0	1	0	0	0	0	1	1	3
0	0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	0	0	0	0	1	0	1	5
0	1	0	0	0	0	0	0	1	1	0	6
1	0	0	0	0	0	0	0	1	1	1	7

$Y_0 = I_1 + I_3 + I_5 + I_7$

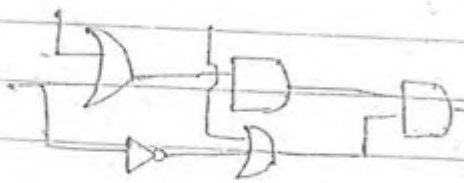
$Y_1 = I_2 + I_3 + I_6 + I_7$

$Y_2 = I_4 + I_5 + I_6 + I_7$

Previous Q's

1) (d) 2) (a) 3) (a) 4) (b) 5) $\bar{x}+y+\bar{z}$ 6) c 8) (a)

9) (d) 10) 12) c 13) (b) 14) (b) 16) (A) $I_1=1, I=B$.



17) (d) 18) c

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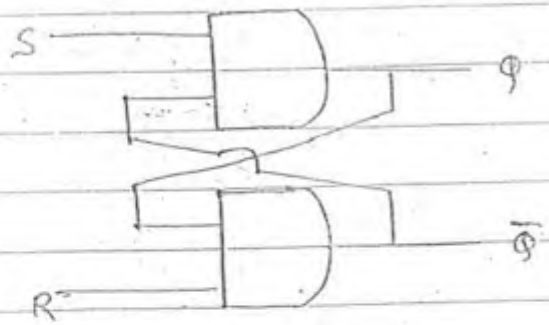
Sequential Circuit

☆ Flip-flop :→

i) It is a basic memory element
ii) F.F can store 1 bit
iii) FF have two o/p which are complementary to each other.
iv) F.F have two stable state hence it is known as bistable multivibrator.

- S-R Latch → NAND / NOR
- SR FF, JK FF, D FF, T FF → Ckt, Truth table, Characteristic table, Characteristic equation, Excitation table.
- Conversion from one FF to other
- Sample circuit

1 SR latch using NAND Gate :→



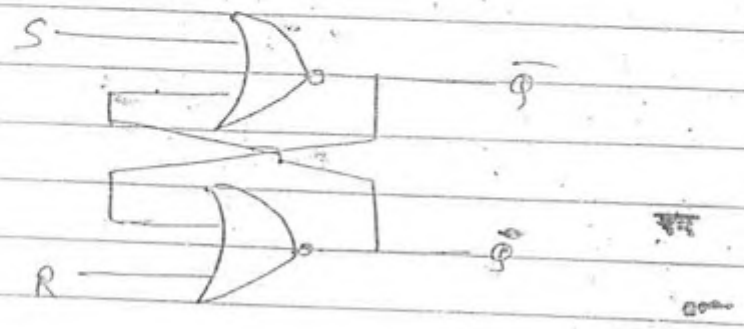
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Enable → 1
Disable → 0

S	R	Q
0	0	Invalid ($Q=\bar{Q}=1$)
0	1	1
1	0	Previous state ($Q=1, \bar{Q}=0$ or $Q=0, \bar{Q}=1$)
1	1	

In S-R latch, if both gates are enable, o/p remains in previous state and if both are disable the o/p remain in invalid

2. SR - Latch using NOR Gate :→



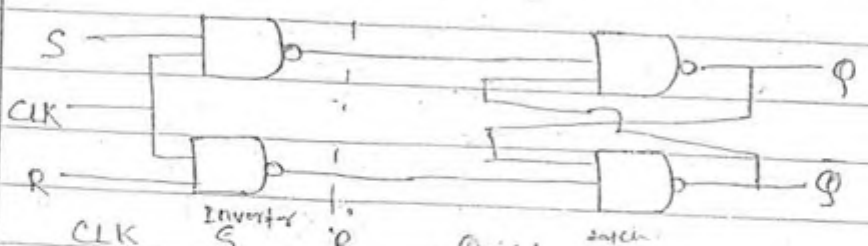
A	B	Y	S	R	Q
0	0	1	0	0	Previous State.
0	1	0	0	1	0
1	0	0	1	0	1
1	1	0	1	1	Invalid.

Enable → 0

disable → 1.

→ S-R latch is used to eliminate switch bouncing.

3. S-R flip-flop :→ [using NAND]



CLK	S	R	Qn+1	
0	X	X	Qn	→ HOLD
1	0	0	Qn	
1	0	1	0	→ Reset
1	1	0	1	→ Set
1	1	1	Invalid → unused.	

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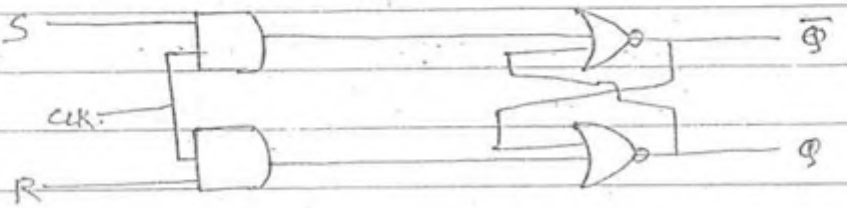
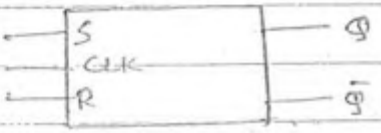
S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Invalid.

4 S.R Flip-flop using NOR gate :→





→ Characteristic Table :→

	S	R	Q_n	Q_{n+1}
Q_n = 0	0	0	0	0
	0	0	1	1
	0	1	0	0
	0	1	1	0
	1	0	0	1
	1	0	1	1
	1	1	0	x
	1	1	1	x

→ Characteristic Equation :→

S \ $Q_n\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
$\bar{S}$		1	
S	1	1	x	x

$$Q_{n+1} = S + \bar{R}Q_n \quad \& \quad S \cdot R = 0$$

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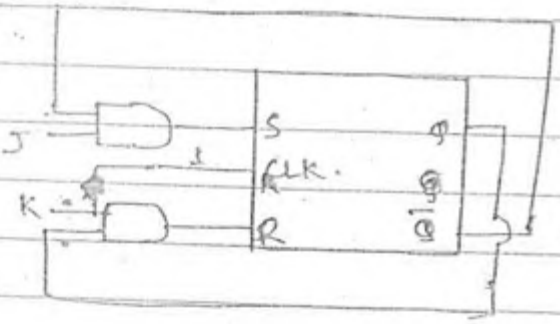
→ Excitation Table :→

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Disadvantage :-

→ Invalid State is present When S & R I/P are 1.
To avoid this J-K Flip-Flop is used.

5 J-K Flip-Flop :→



CLK	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$

J	K	Q_{n+1}	
0	0	Q_n	→ Hold.
0	1	0	→ Reset
1	0	1	→ Set
1	1	$\bar{Q}_n$	→ Toggle.

$S = J\bar{Q}$
$R = KQ$

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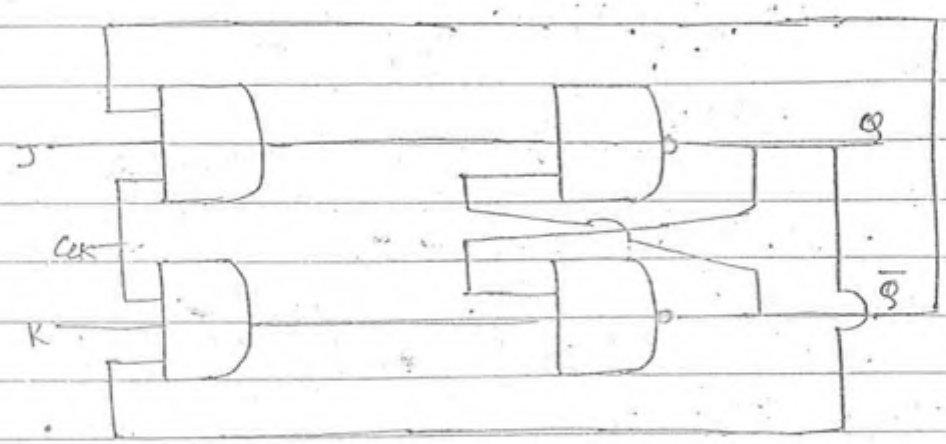
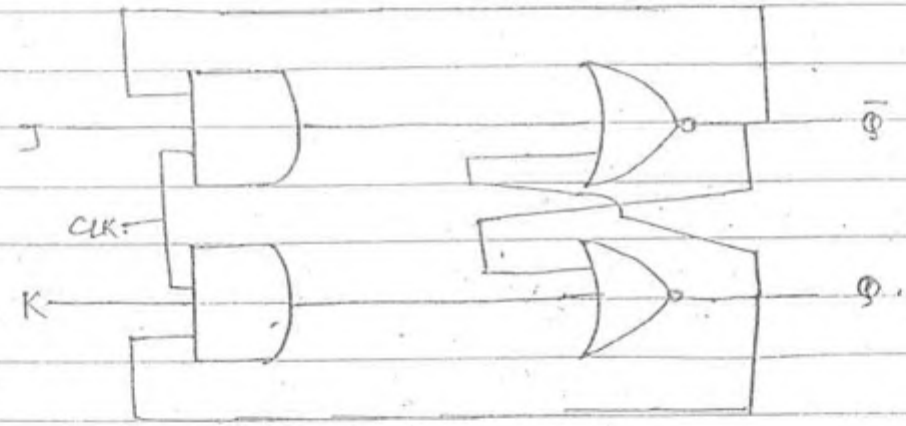
→ J-K Flip-Flop Using NAND Gate :→



→ J-K Flip-Flop Using NOR Gate :—



→ Characteristic Table (J-K F-F) :→

J	K	Q_n	Q_{n+1}	
0	0	0	0	Q_n
0	0	1	1	
0	1	0	0	0
0	1	1	0	
1	0	0	1	1
1	0	1	1	
1	1	0	1	$\bar{Q}_n$
1	1	1	0	

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→ Characteristic Equation :→

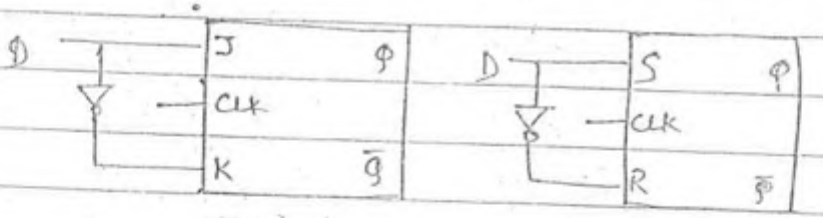
J \ KQn	$\bar{K}Q_n$	$\bar{K}\bar{Q}_n$	KQ_n	$K\bar{Q}_n$
$\bar{J}$		1		
J	1	1		1

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

→ Excitation table :→

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

6. D- Flip-Flop :→ [Transparent Latch]



$J = D \; ; \; K = \bar{D}$

$S = D \; ; \; R = \bar{D}$

→ Truth table.

CLK	D	Q_{n+1}
0	X	Q_n
1	0	
1	1	1

D	Q_{n+1}
0	0
1	1

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→ Characteristic table :→

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

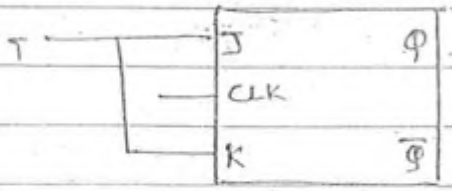
$$Q_{n+1} = D$$

D-Flip-Flop is also called transparent latch.

→ Excitation table :→

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

7 T-Flip-Flop :→ [Toggle Flip-Flop]



$$J = K = T$$

CLK	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$\bar{Q}_n$

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

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→ Characteristic Table :→

	T	Q_n	Q_{n+1}
Q_n	0	0	0
	0	1	1
$\bar{Q}_n$	1	0	1
	1	1	0

$$Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n = T \oplus Q_n$$

→ Excitation table :→

Q_n	Q_{n+1}	T
0 →	0	0
0 →	1	1
1 →	0	1
1 →	1	0

NOTE :-

	J	K	Q_{n+1}	
S-R	0	0	Q_n	
	0	1	0	> D-F-F. → T-F-F.
	1	0	1	
	1	1	$\bar{Q}_n$	

Therefore J-K f-f is a universal F-F.

Excitation Table :-

Q_n	Q_{n+1}	S	R	J	K	D	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

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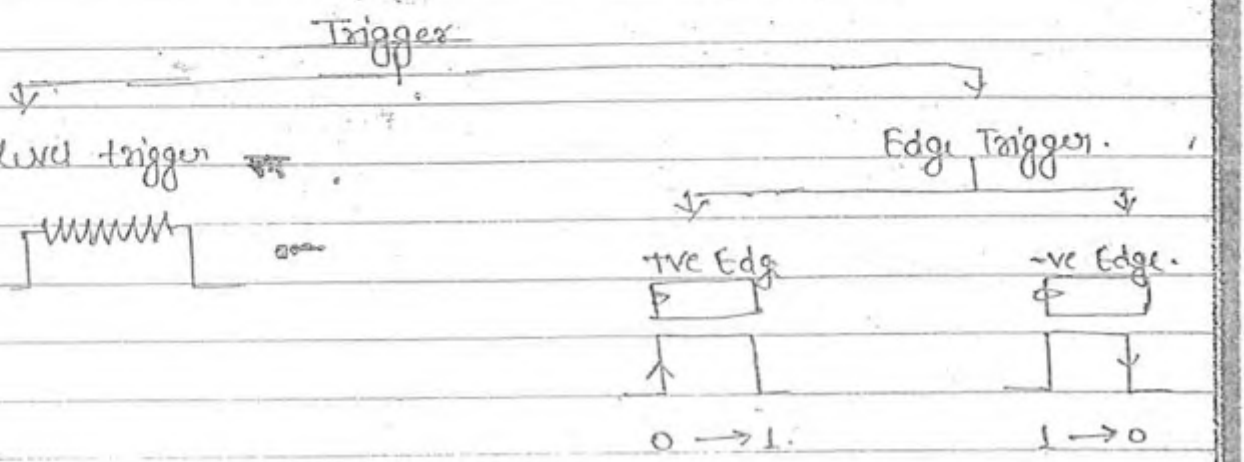
→ Characteristic Equation.

$Q_{n+1} = S + \bar{R}Q_n$

$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

$Q_{n+1} = D$

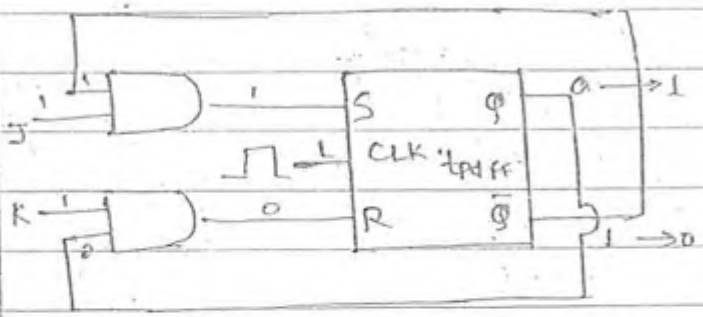
$Q_{n+1} = T \oplus Q_n$

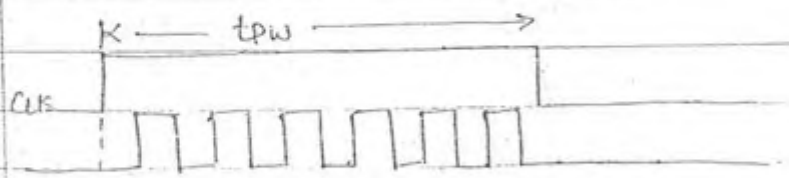


→ In level trigger ckt O/P may change many times in single clk

→ In edge triggered ckt o/p will change only once in single clk.

✡ Race-Around condition





$t_{pdFF} << t_{pw}$

$J = K = 1$

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→ In J-K FF race around condition occurs when J & K I/P are 1 & $t_{pd\,FF} << t_{pw}$.

→ During race around O/P will change many time in a single clk even if I/P is constant.

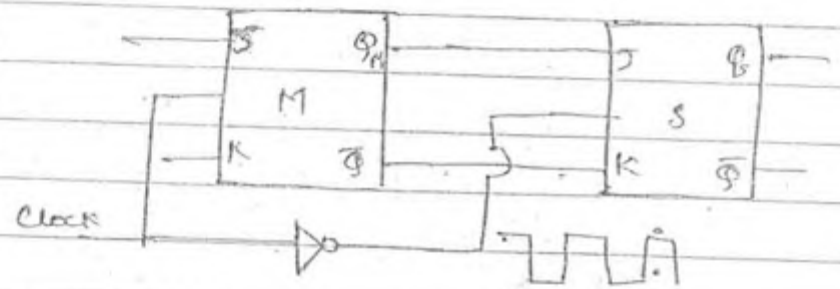
→ Condition to avoid race around:

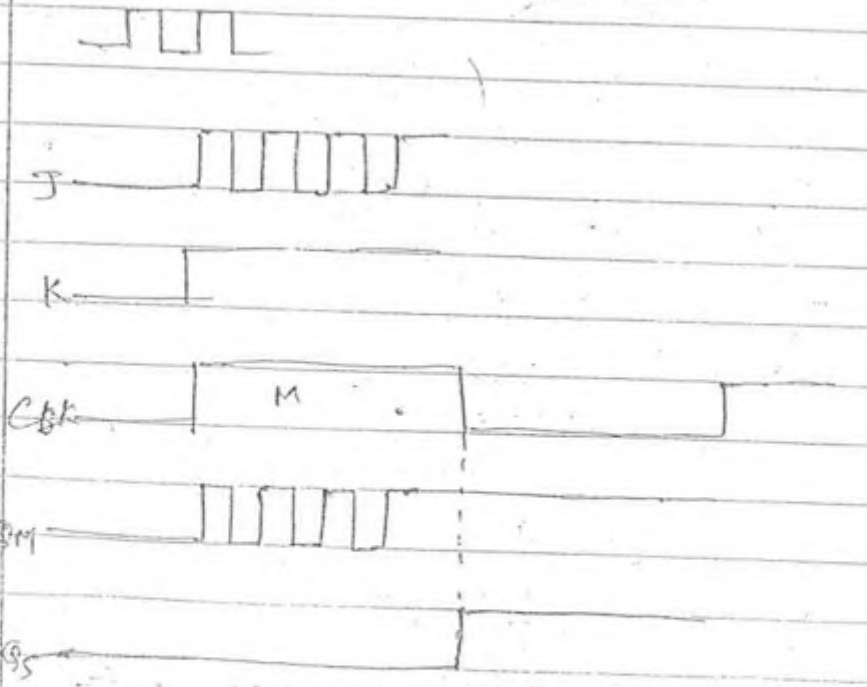
$$t_{pw} < t_{pd\,FF} < T_{clk}$$

$T_{pw} < t_{pd\,FF} < T_{clk}$

→ To avoid race-around condition Master Slave JK ff is used

→ Master Slave J-K Flip-flop :→





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i) In Master Slave F-F, O/P will changes only when Slave O/P is changing.
ii) In Master Slave F-F, Master is level triggered & Slave is edge triggered.

☆ Conversion of one F-F to other :→

1) JK to DFF :→

Procedure

i) Required F-F characteristic table.
ii) Available F-F excitation table.
iii) Write logical expression for excitation.

D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

D \ Q_n	$\bar{Q}_n$	Q_n
$\bar{D}$	0	X
D	1	X

D \ Q_n	$\bar{Q}_n$	Q_n
$\bar{D}$	X	1
D	X	

$J = D$. $K = \bar{D}$

2) S-R to JK FF :-

$S = J\bar{Q}$

$R = KQ$.

3) SR to D :-

$S = D$

$R = \bar{D}$

4) SR to TF·F :-

$S = T\bar{Q}$

$R = TQ$.

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5) JK - SR FF :-

$J = S$

$K = R$

6) J.K - T F.F :→

$J = K = T$

7) D to S.R F-F :→

$D = S + \bar{R}Q$.

8) D to J-K :→

$D = J\bar{Q} + \bar{K}Q$.

9) D to T :→

$D = T \oplus Q$.

10) T to S.R :→

$T = S\bar{Q} + RQ$.

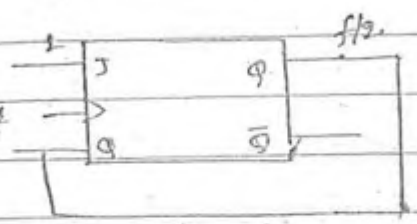
11) T to J.K :→

$T = J\bar{Q} + kQ$.

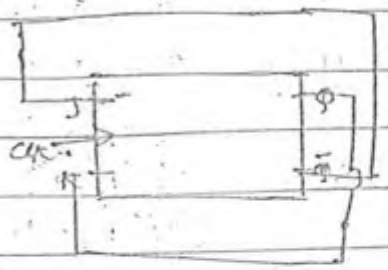
12) T to D :→

$T = D \oplus Q$.

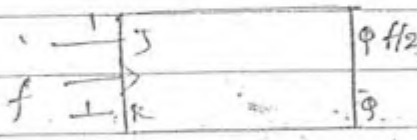
Q) a) i) d



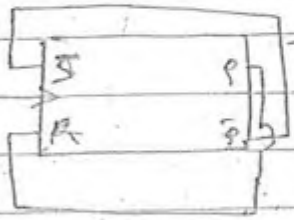
ii)



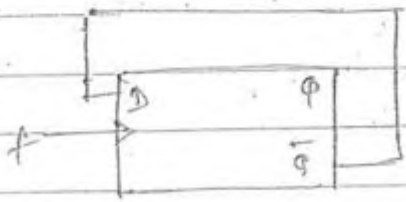
iii)



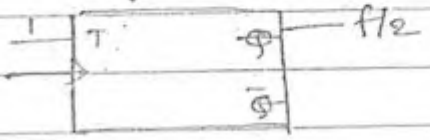
iv)



v)



vi)



Register

→ Register are used to ~~used~~ store group of bit.

→ To store n bit n-bit f-f are cascaded in register.

→ Types of Register :→

1) SISO [Serial In Serial out] :→

2) SIPO [Serial In Parallel out] :→

3) PISO [Parallel In ~~Parallel~~ Serial out].

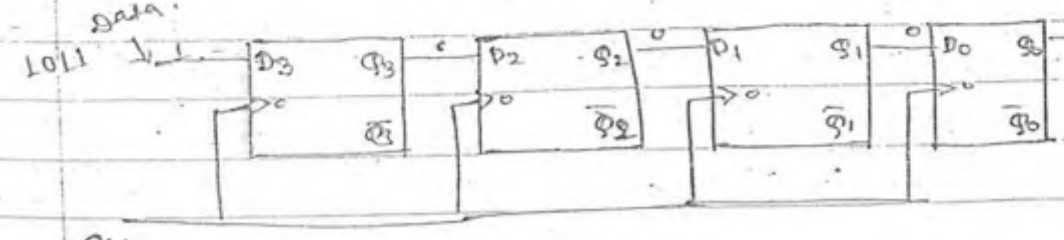
4) PIPO [Parallel In Parallel out].

→ Depending upon Application Register can be classified into

A. Shift Register.

B. Storage Register

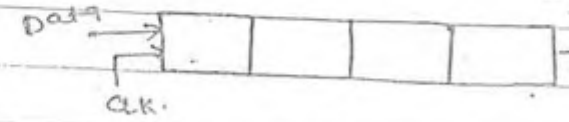
1) SISO :→



Data	$Q_3 Q_2 Q_1 Q_0$	clk.
1011	0 0 0 0	0
	1 0 0 0	1
	1 1 0 0	2
	0 1 1 0	3
	1 0 1 1	4

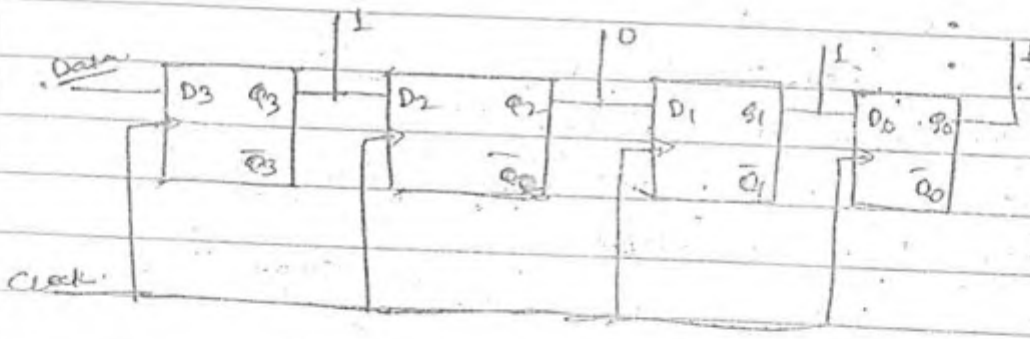
→ In SISO register to store n bit data it require n clock pulse.

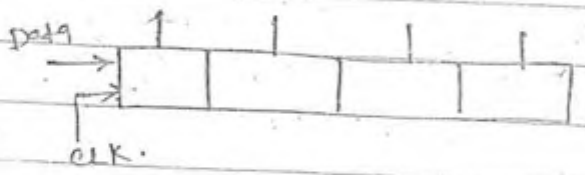
→ To provide a n clock pulse delay to the S/P data.



→ To provide n-bit data serially out it requires (n-1) pulse.

2. SIPO : →





→ In SIPO register, To provide n-bit data serially in it require n clock pulse and to provide parallel O/P 0 clock pulse are required.

→ Serial Data → Temporal code.
Parallel data → Spacial code.

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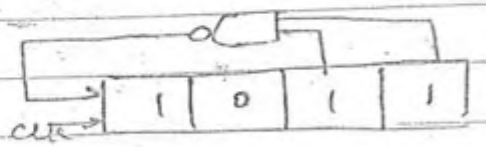
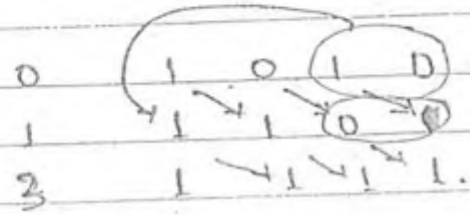
→ SIPO is used to convert temporial code to spacial code.

Q The ckt shown in fig. is 4 bit SIPO which is initially coded with 1010 of 3 clk pulses are applied then the data of the register is

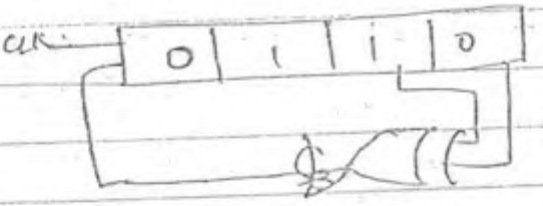
a) 1010 b) 1101 c) 1111 d) 0000.





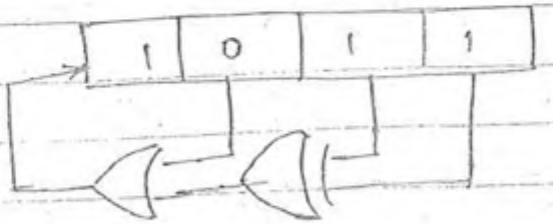
web 8 c)

a)



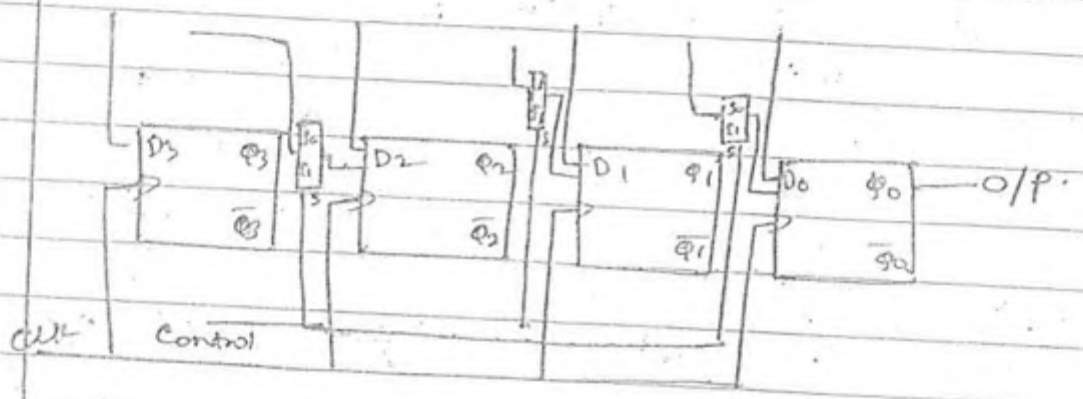
JEB 2010

Q The ckt shown in fig is 4 bit SIPO which is initially coded with 1011. If clk pulses are applied continuously. After how many clock pulses the data given is 1011



clk	Q_3	Q_2	Q_1	Q_0
0	1	0	1	1
1	0	1	0	1
2	1	0	0	1
3	1	1	0	0
4	1	1	1	0
5	0	1	1	1
6	1	0	1	1
7				

3. PISO :→



Control = 0 → P.I

1 → Serial O/P

→ In PISO register, To provide parallel in we require one CLK pulse & to provide serial o/p it require (n-1) clk pulse.

→ PISO can be also used to convert special code to temporial code.

→ In PISO

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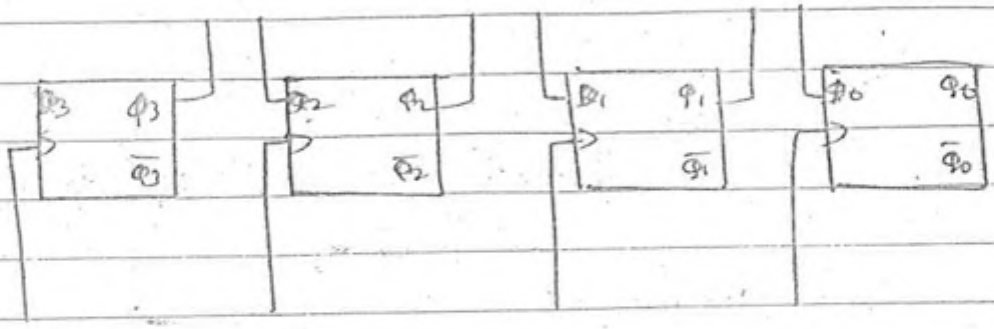
A) PIPO :→



PIPO is used for storage register.

control = 1 → Parallel In. (1 clock pulse req.)
0 → Parallel out. (0 " " ").

	I/P	O/P
SISO	n	n-1
SIPO	n	0
PISO	1	n-1
PIPO	1	0

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Each shift register is to provide multiple the data by (2)

If n shift left operation will

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Counters:

→ It is basically used to count no. of clock pulse are applied.

→ It can be also used in frequency divider.

i) Frequency Divider.
ii) Time measurement
iii) Frequency measurement
iv) Range measurement
v) Pulse width.
vi) Wave form generation.

→ With n f f max^m possible state in a counter = 2^n.

Let N = No of state.
n = No. of flip-flop.

$$N \leq 2^n$$

$$\Rightarrow n \geq \log_2 N$$

→ Depending upon clock pulse apply counters are classified as

1) ASynchronous counter
i) Different ff are applied in different clock pulse.
ii) Slower
iii) Operating with fixed count sequence → up. → Down.
iv) Decoding errors
v) a Ripple counter

2) Synchronous counter.
i) All f·f are applied with same clock pulse.
ii) Faster.
iii) Any count sequence is possible.
iv) No Decoding errors
v) Ex→ Ring counter.

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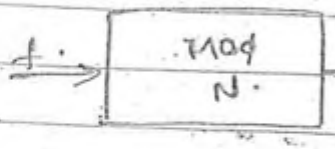
☆ Modulus Counter :→

No. of states used in a counter is called modulus counter.

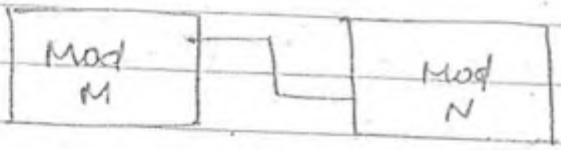
Ex Mod 5 → 5 state.



Q A decade counter is applied with a clock freq. of 10MHz then o/p frequency is

Sol: $\frac{10}{10} = 1MHz$

→ Let M and Mod N counters are cascaded then it acts as Mod MN counter.



Mod MN.

1) Ripple counter
2) Non binary ripple counter
3) Ring counter
4) Thornton counter
5) Synchronous series carry
6) Synchronous parallel carry.
8) Synchronous counter Design & Analysis.

} imp for PSU/ESE/GATE

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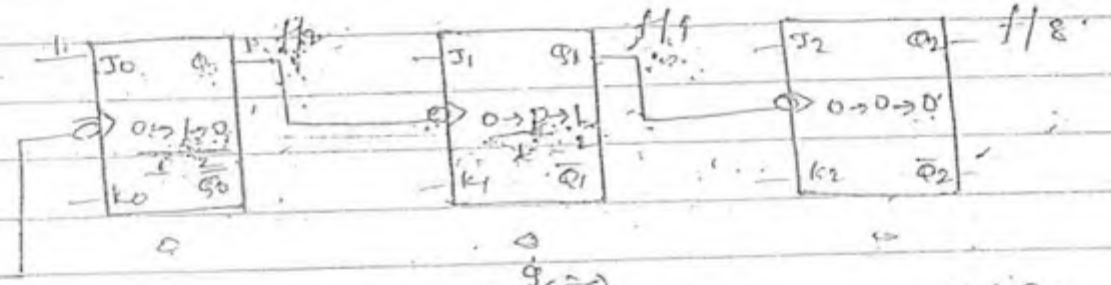
1) Ripple Counter :→

→ It is a asynchronous counter
→ Different clock pulse
→ Toggle mode.
→ In ripple counter only one F.F is applied with external clock & other FF clocks is from previous F.F o/p (Q or $\bar{Q}$)
→ In ripple counter the F.F applied with external clk will acts as LSB bit

→ 3-bit Ripple counter :→ [up counter]



CLK 1→0 1→0 0→0

$Q_1 = 0$

$Q_1 = 1$

LSB 0 1 MSB

In the ckt shown in fig $\bar{Q}_0$ toggle for every clk pulse Q_1 change when Q_0 is changing from 1 → 0 and Q_2 change when Q_1 is change from 1 → 0

Q_0 → every clock
Q_1 → Q_0 → 1 → 0
Q_2 → Q_1 → 1 → 0

Truth table

CLK	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

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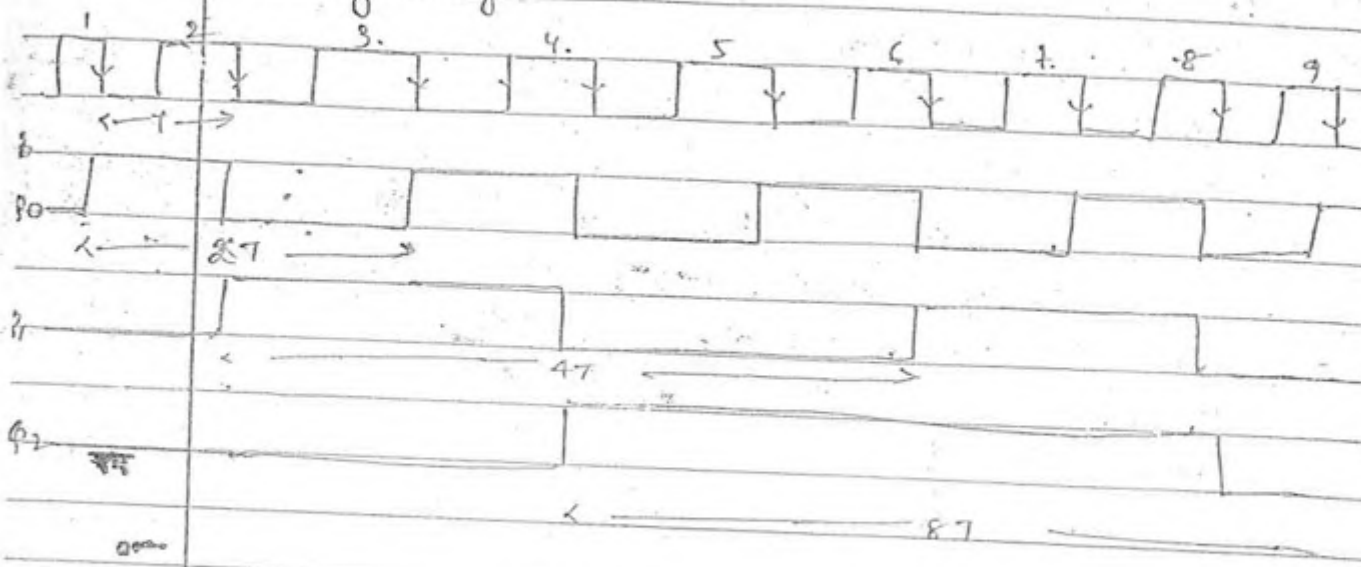
→ Timing Diagram :→



$T_{clk} \geq n t_{pdFF}$.

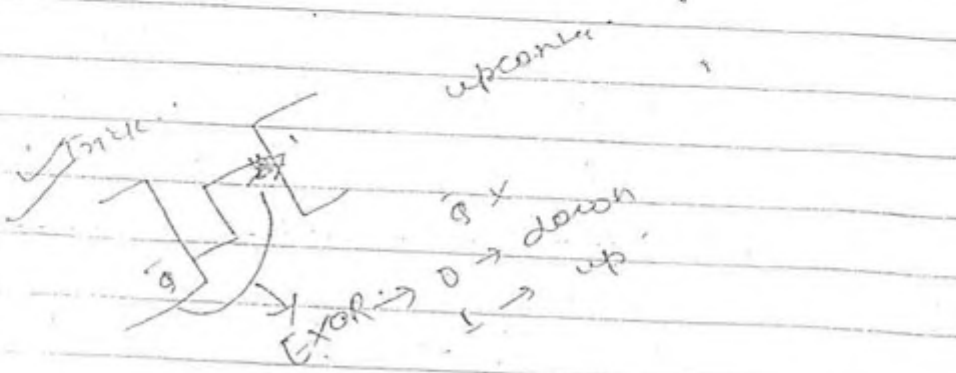
→ In a n bit ripple counter propagation delay of each ff is t_{pdff} then time period of clk

$$T_{clk} \geq n t_{pdff}.$$

$$f_{clk} \leq \frac{1}{n t_{pdff}}.$$

$$f_{max} = \frac{1}{n t_{pdff}}.$$

W.B
30 (d)
32 (b)



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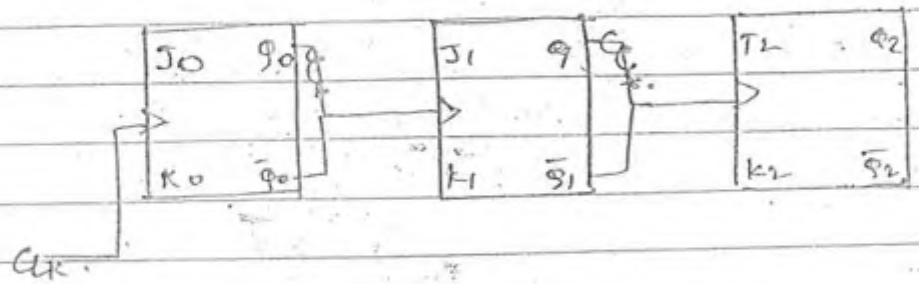
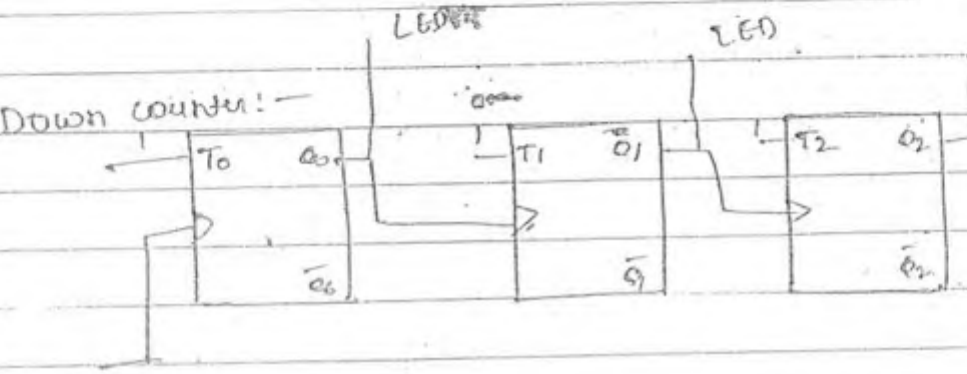
→ -ve edge triggered, $\bar{Q}$ as clock → up counter
+ve edge triggered $\bar{Q}$ as clock → up counter



→ Down counter:-



The ckt shown in fig Q_0 toggle for every clk pulse, Q_1 toggle when Q_0 change from 0 → 1 ~~when~~ Q_2 toggle when Q_1 change from 0 → 1.

Q_0 → Toggle for every clk pulse.
Q_1 → " when Q_0 → 0 → 1
Q_2 → " " Q_1 → 0 → 1

clk	Q_2	Q_1	Q_0	
	0	0	0	000
1	1	1	1	001 → decoding error or Transient
2	1	1	0	011
3	1	0	1	111
4	1	0	0	
5	0	1	1	
6	0	1	0	
7	0	0	1	
8	0	0	0	

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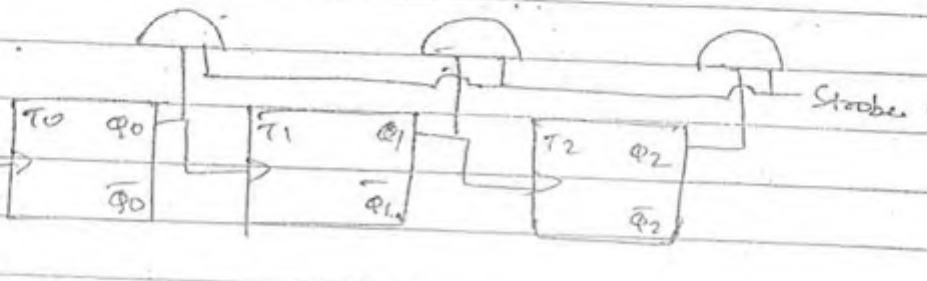
→ +ve edge triggered $\bar{Q}$ as clock → Down counter
-ve edge triggered $\bar{Q}$ as clock → Down counter.

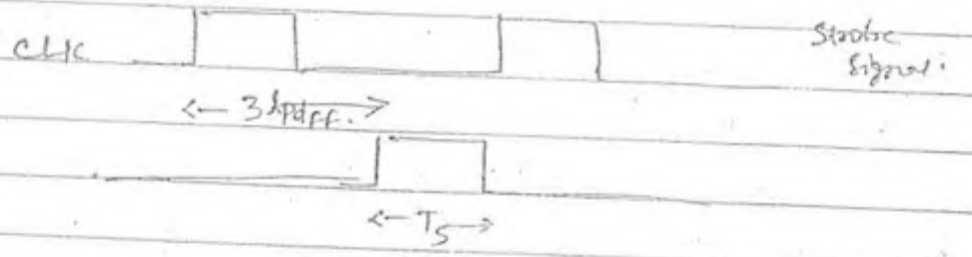
WB 24 b) Up counter.

✱ Decoding Error :→

→ Decoding errors are transient states representing ripple counter due to propagation delay.

→ To avoid decoding error strobe signal are used





$T_{CLK} \geq n t_{pdFF} + T_S$.

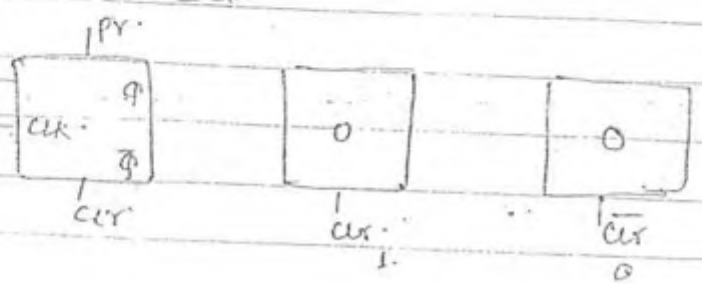
→ In ripple counter with n FF maximum possible state $= 2^n$.

→ S, R, J, K, D, T → Synchronous I/P.

→ Clear, Preset → Asynchronous I/P.

→ Clear → Reset.

Preset → Set.



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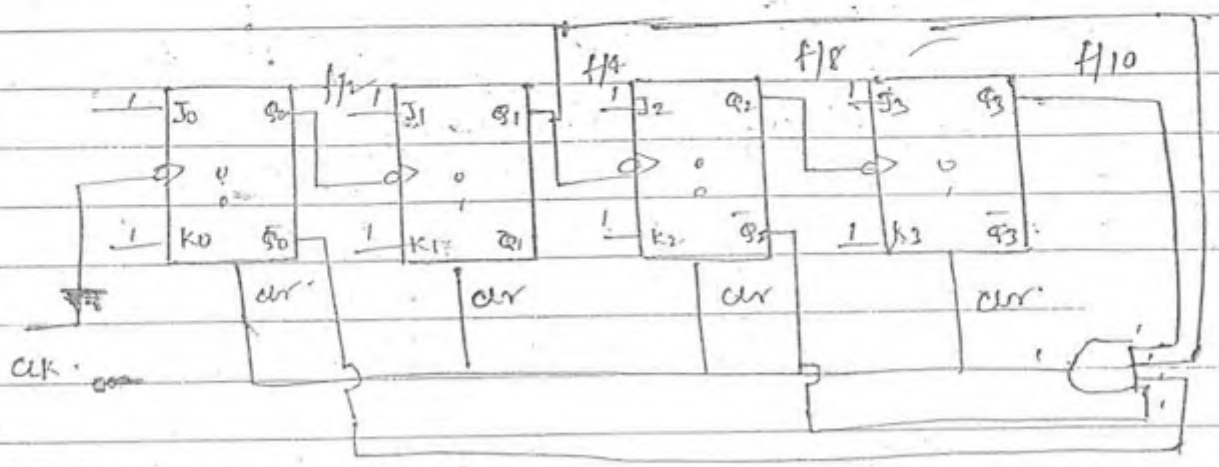
* ~~Non~~ binary ~~Ripple~~ ~~counter~~

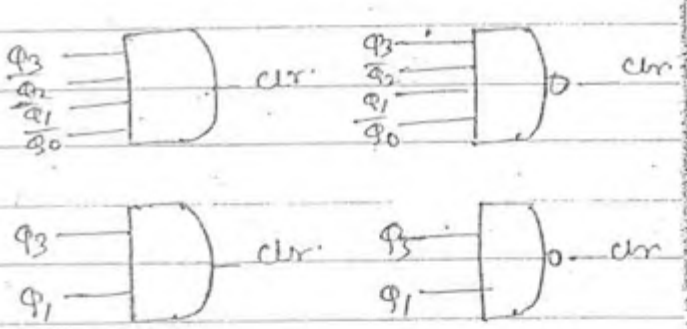
2 Non binary Ripple counter.

3 BCD counter [Decade counter] :→



CLK	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0 ← 1010

$Q_3 \bar{Q}_2 Q_1 \bar{Q}_0$



→ All BCD counter are decade counter but decade counter is not necessarily viceversa.

WB. 15 (a) $8 \times 2 \times 5 = 80$ $\quad \frac{12\,MHz}{60} = 200\,kHz$

16 (b).

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→ Asynchronous counter.

1) Toggle Trigger → +ve
→ -ve.

2) clock. → Φ
→ $\bar{\Phi}$.

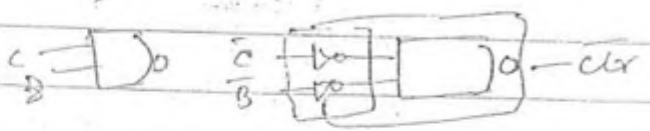
3) Counter → up
→ Down.

4) Preset/clear clear → 000
Preset → 111

5) Decoding error.

W.D 18) (A)
i) +ve edge 111 ✓
ii) Φ as clock. 110 ✓
iii) Down. 101 ✓ } 5
iv) preset = 1111 101 ✓
010 ✓ 111 ✓
111 ✓ ∴ Mod 5 counter

22/23 (C) f/10



Bobbed NAND gate = OR gate.

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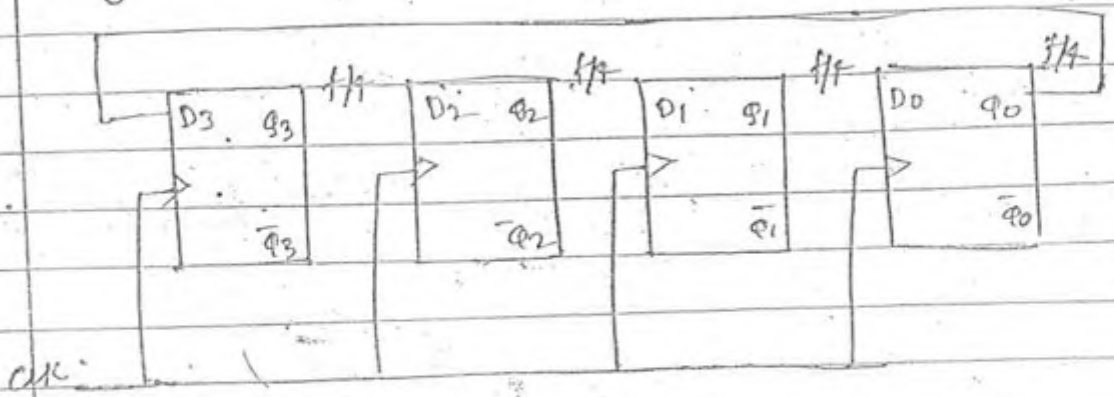
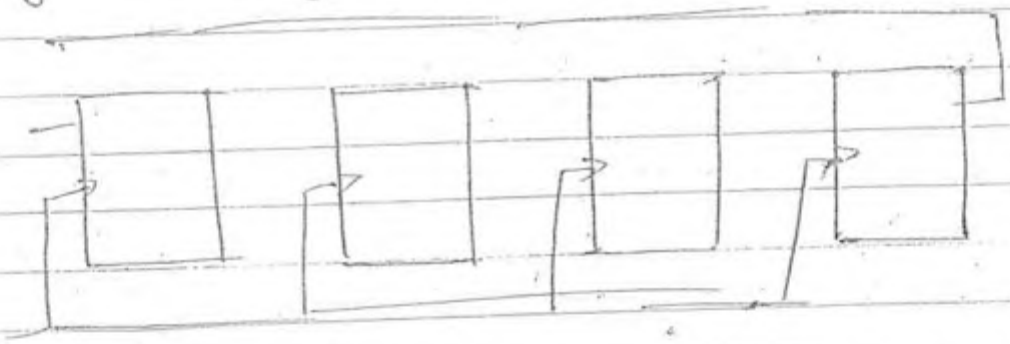
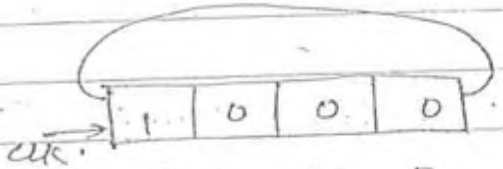
3 Ring Counter :→



→ It is a shift register
→ In this last FF O/P is connected to the first FF I/P.
→ In ring counter only one FF O/P is high & remaining FF are low.



Clock	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
7	0	0	1	0
8	0	0	0	1



0 1 0 0
0 0 1 0
0 0 0 1
1 0 0 0

→ 4 bit ring counter = 4 state.
n bit → n state.
f → f/n.

Unused state = $2^n - n$.

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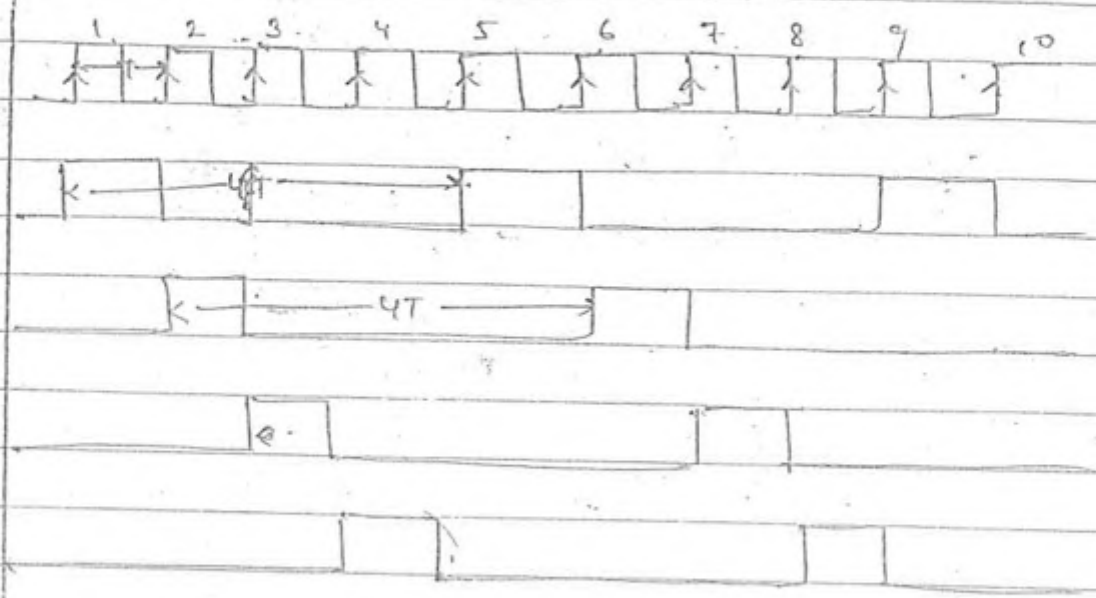
→ Timing Diagram :→



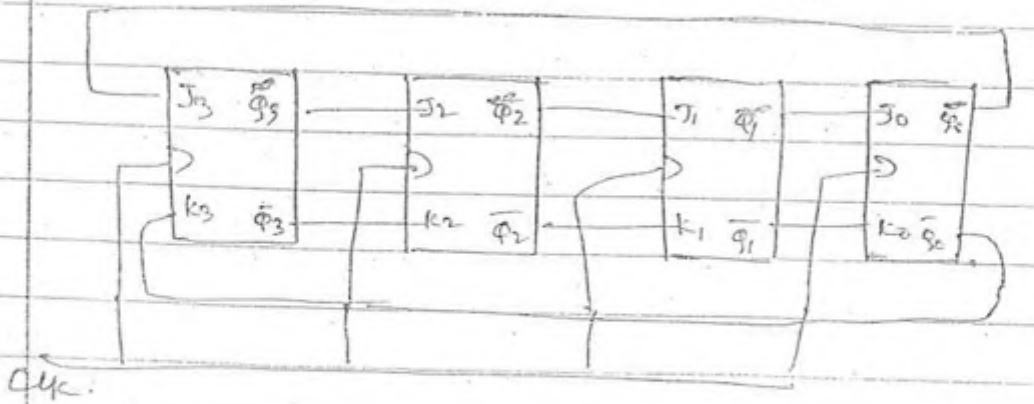
Phase shift b/w generated waveform = $\frac{360}{n}$.

→ It is used in Stepper motor control

→ It is also used ADC

no. of unused state = $2^n - n$.

→ Ring counter using J-K.



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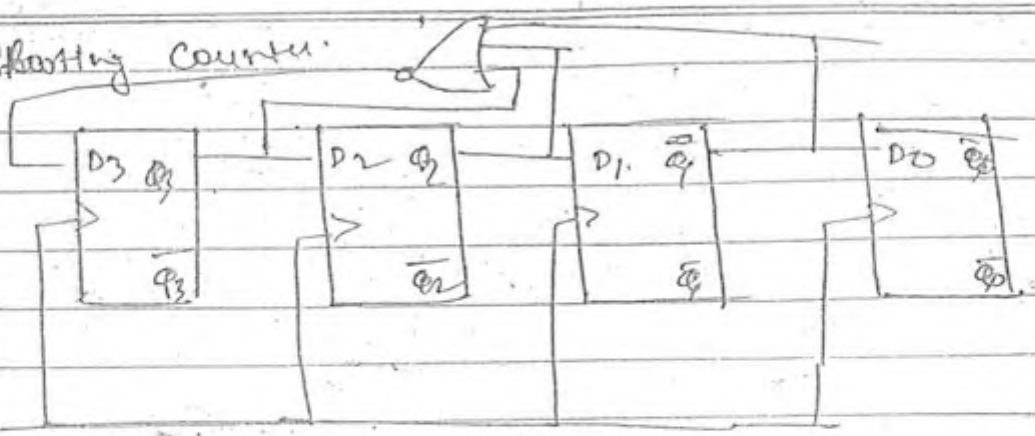
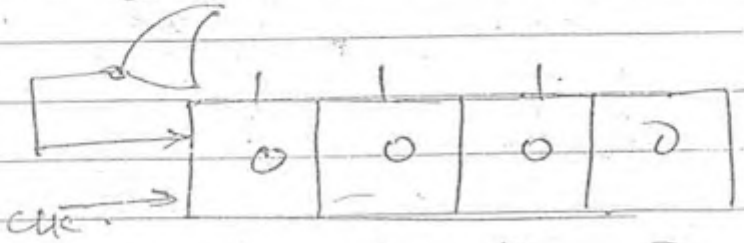
→ Self Starting Counter.

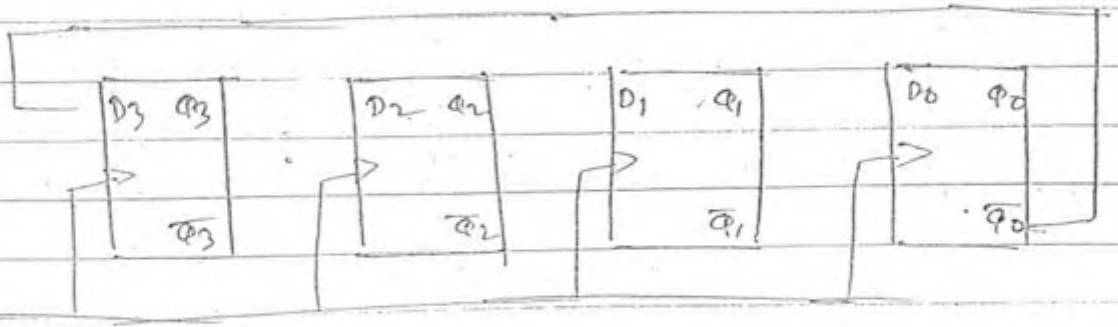


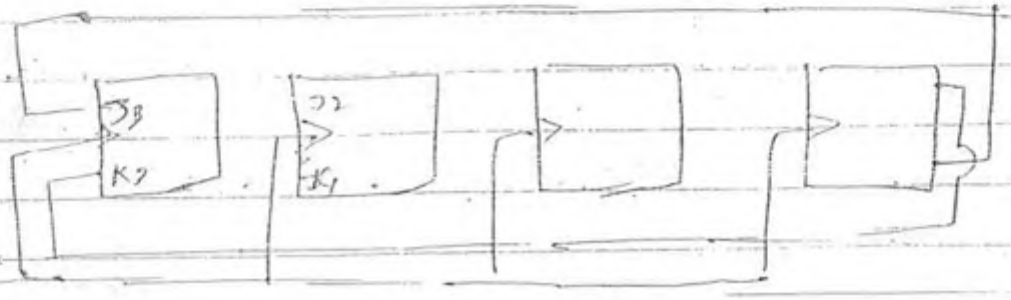


1 0 0 0
0 1 0 0
0 0 1 0
0 0 0 1
0 0 0 0

→ The advantage of ring counter is decoding is easy.
→ To decode no logic gate is required.

→ Thorson Counter :-





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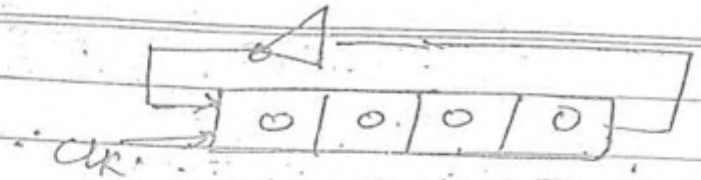

1 0 0 0
1 1 0 0
1 1 1 0
1 1 1 1
0 1 1 1
0 0 1 1
0 0 0 1
0 0 0 0
1 0 0 0
1 1 0 0

4 F.F → 8.
n FF → 2n.

☆ Number System - Codes Data Representation:-

Various Number System

Arithmetic operation → complement
Add, Sub

Various Codes

Data representation → unsined (+ve.
→ sined (+ve, -ve) → Sign magnitude
→ 1's
→ 2's.

Number System And Code

Weighted
Additional Weightage.
Ex.
(3) (2) (1)
10^2 10^1 10^1
Binary.
octal
Decimal
Hexa
BCD code

unweighted.
No weightage.
Ex - Gray code.
Excess-3 code.

A number system with base ✱ radix 'r' ✱ r different digit and they are from (r-1)

Base	Different digit
2	0, 1
8	0, 1 - - - 7.
10	0, 1 - - - 9
16	0, 1, 2 - - - 9, A, B, C, D, E, F.
4	0 - - - - 3
6	0 - - - - 5

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12 0 ---- 9, A, B.

* Decimal to other Conversion:→

$(\cdot)_{10} \longrightarrow (\quad)_r$.

Where r = 0, 1, 2 ---- n

Ex

$(25.625)_{10} = (\quad)_r$.

To convert decimal no. into any other base r divide integer part and multiply fractional part with r.

$(25.625)_{10} = (\quad)_2$

2	25
2	12 - 1
2	6 - 0
2	3 - 0
2	1 - 1
	0 - 1

$= (11001.101)_2$

$0.625 \times 2 = 1.25 \Rightarrow 1$

$0.25 \times 2 = 0.5 = 0$

$0.5 \times 2 = 1.0 = 1$

$(25.625)_{10} = (\quad)_8$.

8	25
8	3 - 1
	0 - 3

$(25)_{10} = (31)_8$

$0.625 \times 8 = 5.0 = 5$

$\therefore (25.625)_{10} = (31.5)_8$

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$(25.625)_{10} = (\quad)_{16}$

16	25	$0.625 \times 16 = 10.000 \rightarrow A$
16	1 - 9	
	0 - 1	$\therefore (19.A)_{16}$ Ans.

$(19)_{16}$

$(254)_{10} = (\quad)_{16}$

16	254	
16	15 - E ↑	$(FE)_{16}$ Ans.
	0 - F ↑	

$(27.4)_{10} = (\quad)_4$

4	27	$0.4 \times 4 = 1.6 \rightarrow 1$	$0.4 \times 4 = 1.6 \rightarrow 1$
4	6 3	$0.6 \times 4 = 2.4 \rightarrow 2$	$0.6 \times 4 = 2.4$
4	1 2	$\therefore (27.4) = (123.\overline{12})_4$	
	0 1		

123

* Others to Decimal number conversion:-

$(x_2x_1x_0.y_1y_2y_3)_r = (\quad)_{10}$

$x_2r^2 \; x_1r^1 \; x_0r^0 \; y_1r^{-1} \; y_2r^{-2} \; y_3r^{-3}$

To convert any other base r to decimal, multiply each digit with positional weightage and then add.

$$x_2r^2 + x_1r^1 + x_0r^0 + y_1r^{-1} + y_2r^{-2}$$

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$(10101.11)_2$ = ( )$_{10}$.

16 8 4 2 1 $\frac{1}{2}$ $\frac{1}{4}$

$1\times16 + 0\times8 + 1\times4 + 0\times2 + 1\times1 + 1\cdot\frac{1}{2} + 1\cdot\frac{1}{4}$

$(21.75)_{10}$.

→ $(57.4)_8$ — ( )$_{10}$

$5\times8 + 7\times1 + \frac{4}{8}$ = $(47.5)_{10}$

→ $(57.4)_{16}$ — ( )$_{10}$.

57.4.

16

$80 + 7\times1 + \frac{4}{16} = (87.25)_{10}$

→ $(BAD)_{16}$ — ( )$_{10}$.

16^2 16 1.

$11\times16^2 + 10\times16^1 + 13\times16^0 = 2989$

$16^0 \rightarrow 1$

$16^1 \rightarrow 16$

$16^2 \rightarrow 256$

$16^3 \rightarrow 4096$.

Ex $(35)_6$ — ( )$_{10}$

6 1

$3\times6 + 5\times1 = 23$

* Octal ↔ Binary

( )$_8$ — ( )$_2$

0 → 000

1 → 001

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Ex $(37.45)_8$ ——— $(\quad)_2$

011 111 . 100 101

* Hex ⟷ Binary.

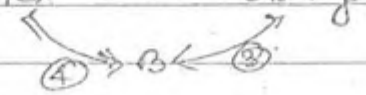
Each digit is represented with 4 bit binary.

$(259A)_{16}$ ——— $(\quad)_2$

0101

$(0010\ 1001\ .\ 1010)_2$

* Hex ⟷ Binary



Ex $(CAD)_{16}$ = $(\quad)_8$

1100 1010 1101 = $(6255)_8$.

* Arithmetic operations :→

Binary — Addition, Substraction, Multiplication.

Octal — Addition, Substraction.

Hex — Addition, Sub.

$(\quad)_r$ — Add, Sub.

→ Binary :-

i) Addition :-

```
  1 1 0 1 1 0
+ 1 0 1 1 0 1
-------------
1 1 0 0 1 1
carry   sum
```

ii) Substraction.

```
  1 1 0 1 1
- 1 0 1 1 0
-----------
  0 0 1 0 1
```

iii) Multiplication :-

1 0 1 0 * 1 0 1

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1010X101 → $(1111)_2 \times (1111)_2$

```
  1010
   101
  ----
  1010
 0000
1010
1100.10
```

```
  1111
  1111
  ----
  1111
 1111
1111
----------
11 11 11 10
1 0 0 0 0.0 1
```

→ 4 = 100 (2)

→ 6 = 110 (3)

W.B. $(10WIZ)_2 \times (15)_{10} = (Y01011001)_2$

```
  10WIZ x 1111
  ------------
  10WIZ
 10WIZ
10WIZ
10WIZ
------
  0.0Z.
```

Z = 1
W = 1
Y = 1

→ Octal :→

0+0 = 0
1+1 = 2
1+2 = 3
:
1+6 = 7
1+7 = 10
7+1 = 10
7+2 = 11
:
7+7 = 16

8 | 10
8 | 1 - 2
0 - 1

8 | 8
8 | 1 - 0
0 - 1

8 | 9
8 | 1 - 1
0 - 1

8 | 14
8 | 1 - 6
0 - 1

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→ 243
212
455

9. 567
243
1032

8 | 11
8 | 1 - 3
0 - 1

Substraction :→
7843
564
1579

→ Hexadecimal System :→

1) Addition :-

1+1 = 2
1+2 = 3
:
1+9 = A
1+A = B.
1+B = C
A+A = 14
10+10
A+B = 15

16 | 20
16 | 1 - 4
0 - 1

16 | 21
16 | 1 - 5
0 - 1

10

Q. 5689
4574
9BFD

ADD 26→1A
DAD 24→18
1 1
188A

13 | 26
13 | 2 0
0 2

11) Substraction :→ 10 16
9743·B
587C
3EBF

16
+11
27
-12
15 = F

19
2
17

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Complements :→

r → (r-1)'s.
→ r's.

B → 1's
→ 2's.

O → 7's.
→ 8's

D → 9's.
→ 10's.

H → F's.
16's.

→ (r-1)'s complement :→

To determine (r-1)'s complement substract given no. from maximum no. possible in the given base ($r^n - 1$)

4 bit → $2^4 - 1$.

→ 1's complement

1 1 1 1 1
1 0 1 1 0 1

0 1. 0 0 1 0

→ 7's complement :→

7 7 7 7
5 6 7 4.
2 1 0 3 Ans

→ 9's complement of Decimal number :-

9 9 9 9
2 6 7 9
7 3 2 0 Ans

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→ F's complement of hexadecimal no.

```
  FFFF
  2689
------
  D976
```

→ r's complement :→

To determine r's complement first to write (r-1)'s complement and then add 1 to LSB (Right-most)

Ex

2's complement → 10100

1's 01011

+1 1

01100

1's 01001·00

+ 0

01001·00

8's Complement

```
  2670
7's 7777
  2670
------
7's 5107
   + 1
------
  5110
```

10's Complement :-

```
  5690
9's 9999
  5690
------
  4309
   + 1
------
  4310
```

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16's Complement:-

5289
F's FFFF
5289
ADD76
+1
AD77 Ans

W.K.T $(11C.D)_{13} = (\quad)_{10}$

$1\times r^2 + 1\times r^1 + C\times r^0 + D\times r^{-1}$ here r=13.

$1\times 169 + 1\times 13 + C\times 1 + D$ = 194 (b)

2) (c) $(FE35)_{16}$ XOR $(CB15)_{16}$.

FE35 → 1111 1110 0011 0101.
1100 1011 0001 0101
0011 0101 0010 0000
3 5 2 0
3520 (c)

3) F's complement (C)

FFFF
2BFD
D402

4) (b) no of 1's = 6
(3)×512 + (7)×64 + (5)×8 + (3).
3753
01 111 101 011 → (9)

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7 (d)
800
11D

0E3

8 (a) $(4)\times 4096 + (9)\times 256 + (7)\times 16 + (5)$

0100 1001 0111 0101

9 (a) 2.3

1.2

10.1

4 | 5	4 | 4	
4 | 1 — 1 ↑	4 | 1 0 ↑	
0 — 1	0 1	

11 135

144

323

6 | 9	
6 | 1 — 3	
0 — 1	

20 (d)

21 $(235)_{R_1} = (565)_{10}$

$(565)_{R_2} = (1065)_{R_2}$

$R_2 < 10$

$R_2 = 10$

$2\times R_1^2 + 3\times R_1 + 5 = 565$

$2\times 256 + 3\times 16 + 5 = 565$ ✓

$2\times 144 + 3\times 19 + 5 \neq 565$

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CODES

1. BCD code:-
2. Excess 3 code.
3. Gray code.

1) BCD [Binary Coded Decimal]:-

i) It is 4-bit code.
ii) Weighted code.
iii) 8421
iv) Each decimal digit is represented with 4 bit.

Decimal	BCD code	Excess 3 code.
0	0 0 0 0	0 0 1 1
1	0 0 0 1	0 1 0 0
2	0 0 1 0	0 1 0 1
3	0 0 1 1	0 1 1 0
4	0 1 0 0	0 1 1 1
5	0 1 0 1	1 0 0 0
6	0 1 1 0	1 0 0 1
7	0 1 1 1	1 0 1 0
8	1 0 0 0	1 0 1 1
9	1 0 0 1	1 1 0 0

Self complement code.

1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1

Invalid BCD code.

⇒ During arithmetic operation if invalid BCD is present then add 6 (0110) to take correct result.

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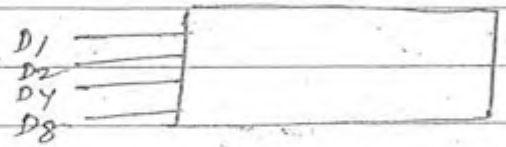
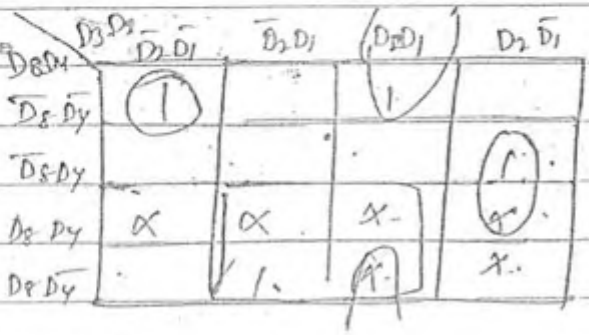
Q A combinational ckt is applied with 4-bit BCD code which is designated as $D_8, D_4, D_2 D_1$. O/P is Y is 1 when I/P BCD is divisible by 3. then the logical expression for Y is



Sol:



$$D_8 D_1 + D_4 D_2 \bar{D}_1 + \bar{D}_4 D_2 D_1 + \bar{D}_8 \bar{D}_4 \bar{D}_2 \bar{D}_1$$

$(839)_{10}$

1000 0011 1001

2> Excess-3-code:—

i> Unweighted

ii> 4 bit code.

iii> BCD + 3 (0011)

iv> Self complument code.

2421
3321
4311
5211

Self complemented & Weighted code.

2+4+2+1 = 9

3+3+2+1 = 9

4+3+1+1 = 9

5+2+1+1 = 9

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2421 Code	Decimal
0000	0
0001	1
0010	2
0011	3
0100	4
1011	5
1100	6
1101	7
1110	8
1111	9

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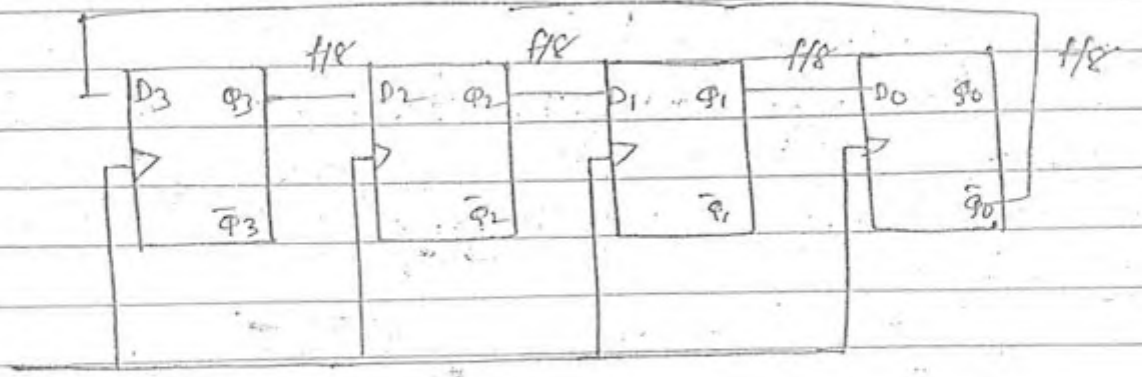
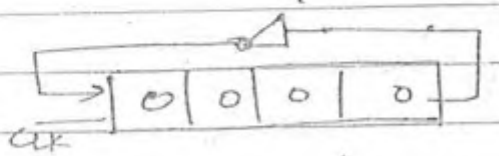
☆ Jhonson Counter :→ [Twisted ring counter or Mobius counter] :-
Creeping counter or walking counter or switch tail counter.





CLK	Q_3	Q_2	Q_1	Q_0	Decoding logic.
0	0	0	0	0	→ $\bar{Q}_3\bar{Q}_0 = \overline{Q_3+Q_0}$
1	1	0	0	0	→ $Q_3\bar{Q}_2$ AND, NOR.
2	1	1	0	0	→ $Q_2\bar{Q}_1$
3	1	1	1	0	→ $Q_1\bar{Q}_0$
4	1	1	1	1	→ Q_3Q_0
5	0	1	1	1	→ $\bar{Q}_3Q_2$
6	0	0	1	1	→ $\bar{Q}_2Q_1$
7	0	0	0	1	→ $\bar{Q}_1Q_0$
8	0	0	0	0	

n FF → 2n States.
no. of unused states = $2^n - 2n$.

Other Name of Jhonson Counter :-
Twisted ring counter
Mobius counter
Creeping counter
Walking Counter
Switch tail counter.

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→ In Jhonson counter to decode each state one two input AND gate / NOR gate.

→ Disadvantage:-

i) Lock out may occur when counter enter into unused state.

→ In. Synchronous counter propagation delay of each FF is t_{pdff} then.

$T_{clk} \geq t_{pdff}$.

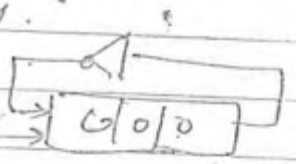
$f_{clk} \leq \frac{1}{t_{pdff}}$.

$f_{max} = \frac{1}{t_{pdff}}$.

W.B

(2) (d) 0 → 01101
1 → 0101
2 → 0100
16 → 0110
32 → 0110
33 → 0101
34 → 0100
35 → 0011
36 → 0010
37 → 0001

(3) (b)



0 → 000
1 → 100
2 → 110
3 → 111
4 → 011
5 → 001
6 → 000

4) (c) ON & OF Period Same → Symmetrical Square wave.

MOD 5 x MOD 2

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→ BCD counter can not use symmetrical count square wave.

15 (a)

16 (a)

14 (c) 4

13) (c)

13 (a)

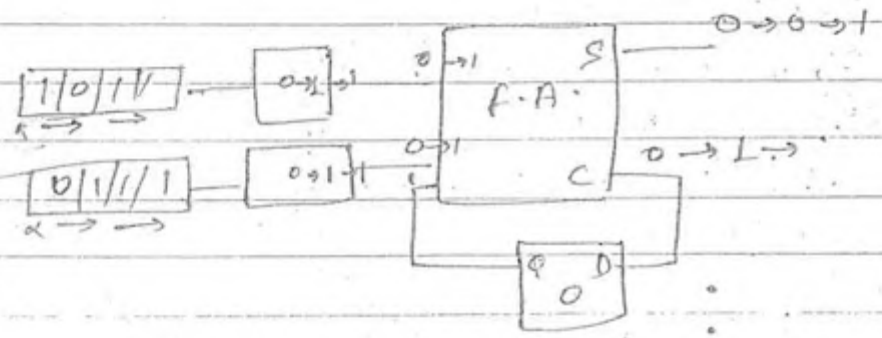
11 (c)

12) $R = \frac{1}{2} \times tpd$

$S = tpd$.

(b)

25



1 0 1 1

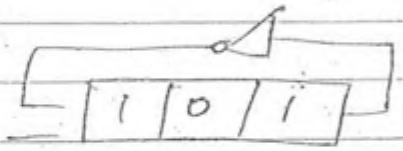
0 0 1 1

1 1

1 1 1 0 $S = 1$

$C = 1$

27 (d)



1 0 1

0 1 0

1 0 1

0 1 0

1 0 1

f/2

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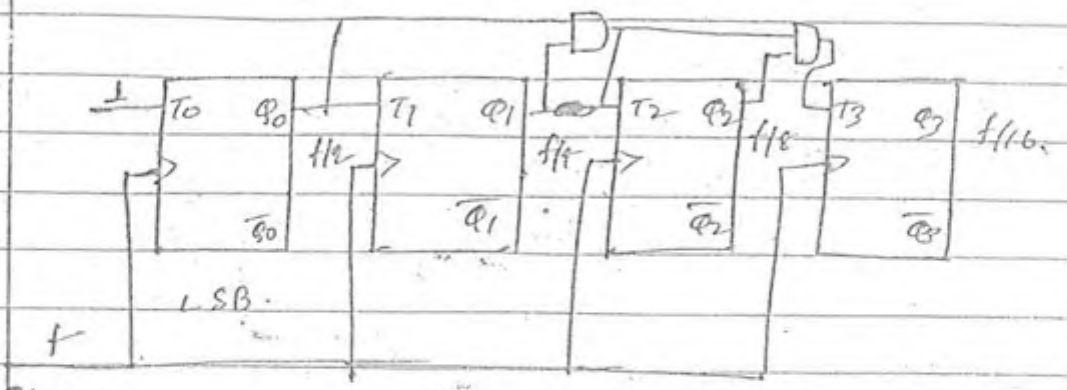
Synchronous Series Carry Counter:→



→ Ckt shown in figure is synchronous series carry up counter.
→ In this counter Q_0 toggle for every clock pulse
Q_1 toggles when $Q_0 = 1$ & clock is applied
Q_2 toggles when $Q_1 Q_0 = 1$ & clock is applied
Q_3 toggles when $Q_2 Q_1 Q_0 = 1$ & clock is applied.

→ Truth table.

CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

$T_{CLK} \geq t_{pdFF} + (n-2)\, t_{pd\,AND}$

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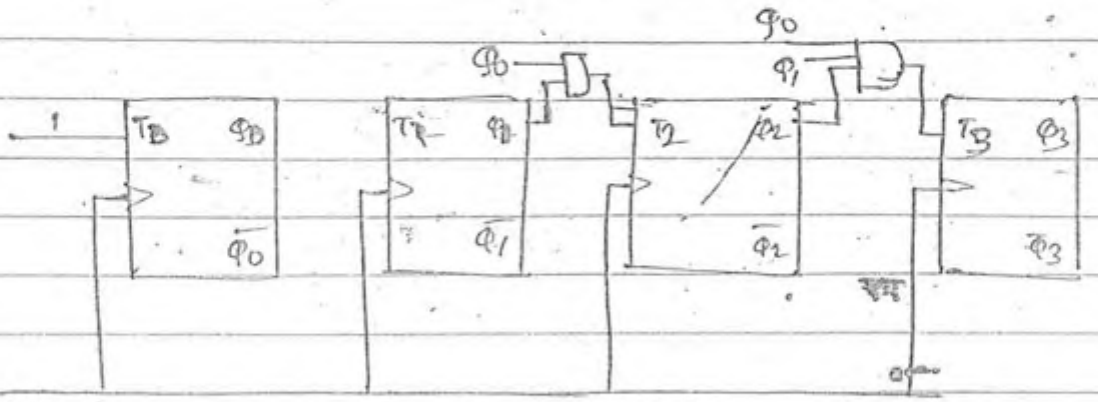
→ To provide down counter use $\bar{Q}$. o/p to the next stage i/p.

☆ Synchronous parallel carry counter.

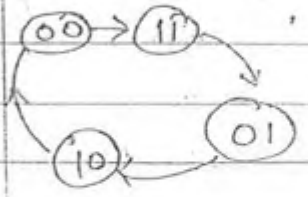


$$T_{clk} = t_{pDFF} + t_{pd\,AND}.$$

→ Synchronous parallel carry counter is faster than synchronous series carry counter.

→ Its operation is same as synchronous series counter.

☆ Synchronous Counter Design for the Given Count Signal :→
Design a synchronous counter for the count signal $0 \rightarrow 3 \rightarrow 1 \rightarrow 2 \rightarrow 0$. using +ve edge triggered DFF.



State diagram.

Sol:

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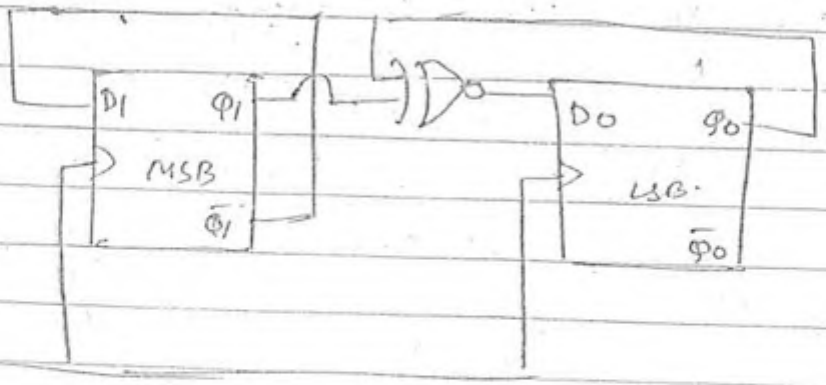
1) Identify no. of F.F & I/P & O/P.
2) Construct State table. excitation.
3) Write logical expression for I/P
4) Minimize.
5) Implement

→ State table.

Present State		Next State		Excitation I/P	
Q_1	Q_0	Q_{1+}	Q_{0+}	D_1	D_0
0	0	1	1	1	1
1	1	0	1	0	1
0	1	1	0	1	0
1	0	0	0	0	0

$$D_1 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0$$
$$= \bar{Q}_1$$
$$D_0 = \bar{Q}_1 \bar{Q}_0 + Q_1 Q_0$$
$$= Q_1 \odot Q_0$$

→ Implementation :-



Ok.

→ using T F.F :-

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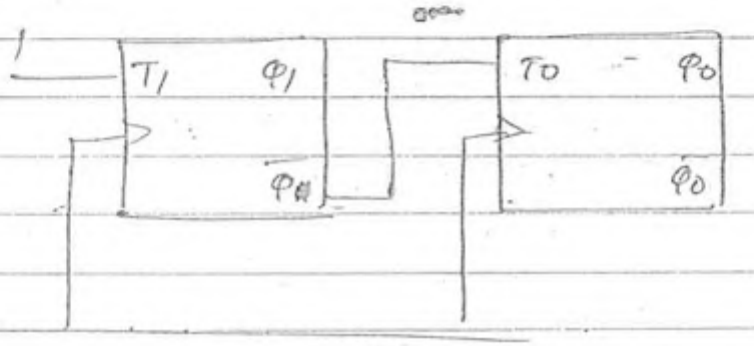
State table: Next State.

Q_1	Q_0	Q_{1+}	Q_{0+}	T_1	T_0
0	0	0	1	1	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	0	1	0

$T_0 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0$

$= \bar{Q}_1$

$T_1 = 1$



Q Design a Synchronous counter for the count sequence
$0 \rightarrow 2 \rightarrow 5 \rightarrow 3 \rightarrow 4 \rightarrow 7 \rightarrow 0$.

Sol: State table:

Present State			Next State		
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
0	0	0	0	1	0
0	1	0	1	0	1
1	0	1	0	1	1
0	1	1	1	0	0
1	0	0	1	1	1
1	1	1	0	0	0
0	0	1	0	0	0
1	1	0	0	0	0

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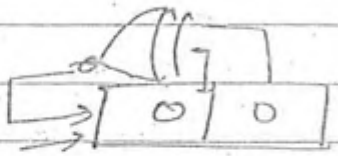
To avoid lock out change unused state to into one of used state in state table.

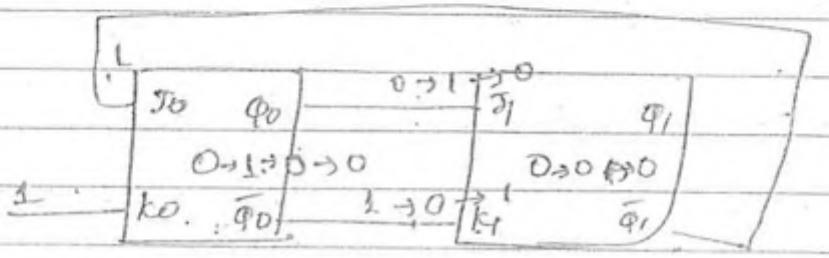
W(27)



	Q_1	Q_0
1 0	0	0
0 1	1	0
0 0	0	0

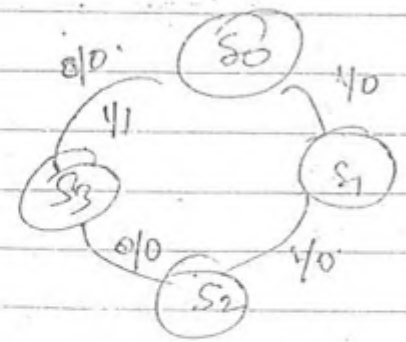
(b)

28



clk	Q_0	Q_1
0	0	0
1	1	0
2	0	1
3	0	0
33	0	0

(10)



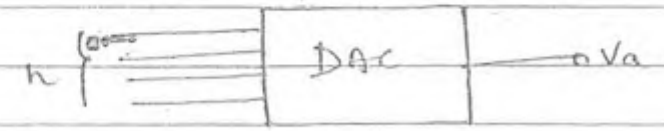
4-bit - 4 state.
↳ 2FF.

31 (a)

ADC / DAC

DAC	ADC
1) Weighted Resistor	1) Counter type
2) R-2R Ladder	2) SAR Type
	3) Flash
	4) Dual Slope integrating type

☆ Digital To Analog Converter (DAC):-



→ Characteristics :→

1) Resolution
2) Analog o/p voltage
3) Full Scale voltage
4) % Resolution
5) Accuracy
6) Linear
7) Monotonic

1. Resolution :→

Resolution of DAC correspond to change in analog voltage for one LSB increment at the I/P

If refrience voltage is given, then resolution of n-bit DTA converter is

$$\text{Resolution} = \frac{V_{ref}}{2^n - 1}$$

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2) Analog o/p voltage :→

> Analog o/p voltage = Resolution x Decimal equivalent of binary data.

Q. In a 4 bit DAC, refrence voltage is 5V and a binary data 1001 is applied then analog o/p voltage is

Sol:

$$V_a = \frac{5}{15} \times 9 = 3 \text{ volt} \quad \text{Ans.}$$

3) Full scale voltage :—

> V_{FS} = Resolution x Max^m Decimal

$$= \frac{V_{ref}}{2^n - 1} \times 2^n - 1$$

$$\Rightarrow \boxed{V_{FS} = V_{ref}.}$$

4) % Resolution :→

> % Resolution = $\frac{\text{Resolution}}{V_{FS}} \times 100$

$$\% \text{ Resolution} = \frac{\frac{V_{ref}}{2^n - 1}}{V_{ref}} \times 100$$

$$\boxed{\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100}$$

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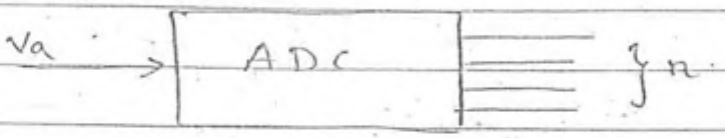
ADC :-



$$\text{Resolution} = \frac{V_{range}}{2^n - 1}$$

$$V_{range} = V_{max} - V_{min}$$

5 Error Accuracy :→

Maximum error acceptable in ADC and DAC is equal to resolution or step size.

$$\%\ \text{Resolution} = \frac{1}{2^n - 1} \times 100$$

$$\text{Dynamic Range} = (6n + 1.76)\ dB \simeq 6n\ dB$$

Resolution

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5) $V_{FS} = 10.24$

$n = 10$

$\text{Resolution} = \frac{10.24}{n} = \frac{10.24}{2^{10}} = \frac{10.24}{1024} = 10\,mV$

error $= \pm 5V$

0 $\xrightarrow{+}$ 50° $\quad \pm 25 \rightarrow 5mV$

25°c $\quad 1 \rightarrow \frac{5}{25} = 200\,\mu V/°c$

6) (a) % Resolution $= \frac{1}{2^n - 1} \times 100 = 0.4$

$\frac{1}{2^n - 1} \approx 0.004$

$\frac{1}{2^8 - 1} \approx \frac{1}{250} = 0.004$

$\therefore$ 8 bit

8) (a) $n = 10$

range $= 5$

$\text{Resolution} = \frac{5}{1023} \approx \frac{5}{1000} \approx 5mV$

16) (b) $n = 12$

% Resolution $= \frac{1}{2^{12} - 1} \times 100 = \frac{1}{4095} \times 100 \approx \frac{1}{4000} \times 100$

$= 0.025$

17) Accuracy (Resolution) $= 10\,mV$

$\frac{5}{2^n - 1} = 10$

$n = 9 \quad , \quad \frac{5}{5000} = 10\,mV$

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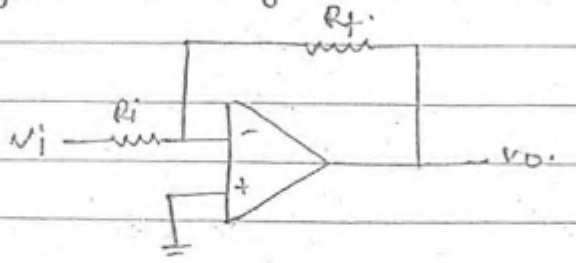
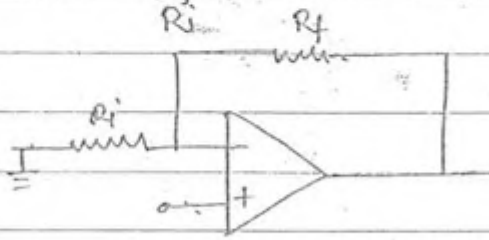
☆ Digital to Analog Converter (DAC) :→

→



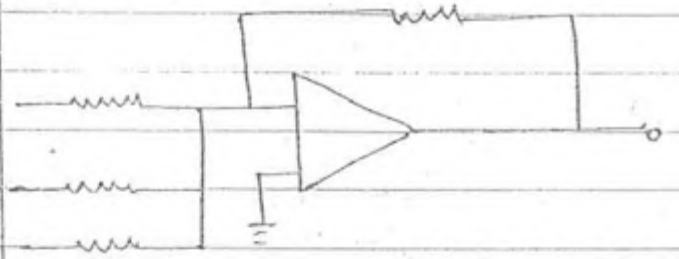
$$V_0 = -\frac{R_f}{R_i} \cdot V_i$$

→



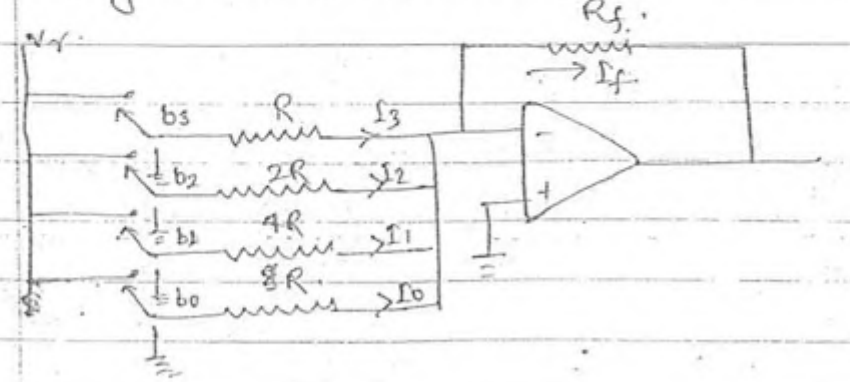
$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_i$$

→



$$V_0 = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \cdots\right)$$

→ Weighted Resistor DAC :→



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$I_3 = \frac{V_r}{R} \cdot b_3$

$I_2 = \frac{V_r}{2R} \cdot b_2$

$I_1 = \frac{V_r}{4R} \cdot b_1$

$I_0 = \frac{V_r}{8R} \cdot b_0$

$I_f = I_3 + I_2 + I_1 + I_0$

$V_0 = -I_f \cdot R_f$

L.S.B Resistance = (2^{n-1}) MSB Resistance

→ Not popularly used.

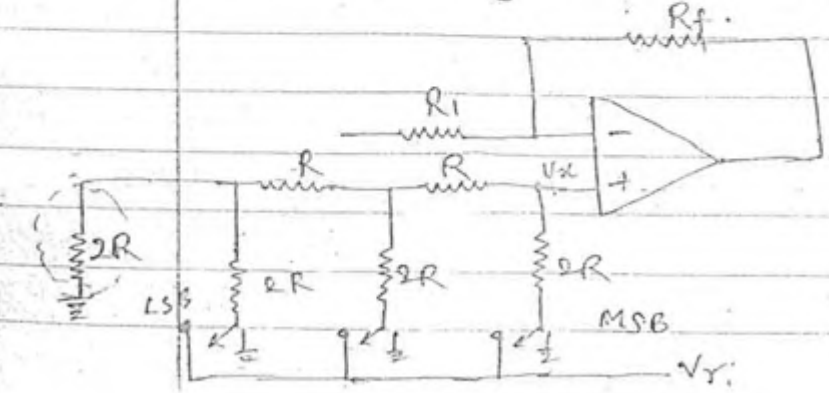
→ In weighted resistor DAC, accuracy is less due to use of different resistor. To avoid this R-2R ladder network is used.

→ R-2R Ladder Network :→

Normal ladder
1) Non Inverting
2) Inverting

Inverted ladder

1) Non Inverting R-2R ladder :→



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$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_x$$

Where V_x = Resolution x Decimal equivalent of binary data.

$$= \frac{V_r}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i$$

$$\therefore \boxed{V_0 = \frac{V_r}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i \times \left[1 + \frac{R_f}{R_i}\right]}$$

= Resolution x Decimal x gain.

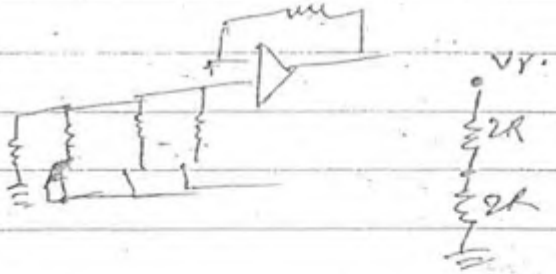
Note:-

b_2 b_1 b_0

$b_2 2^2 + b_1 2^1 + b_0 2^0 = \sum_{i=0}^{n-1} 2^i b_i$

Applying Superposition theorem.

$$V_x = \frac{V_r}{8} \times 1$$



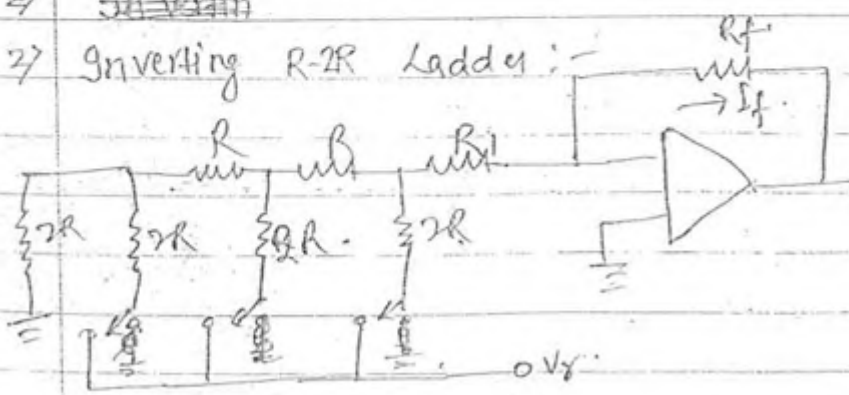
WB

11 $V_0 = \frac{V_r}{2^4} \times 10 \times 8$

$= 5V$

2) ~~Inverting~~

2) Inverting R-2R Ladder :-



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$$V_0 = \frac{V_r}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i \times \left[\frac{-R_f}{R_1+R}\right]$$

= Resolution x Decimal x gain.

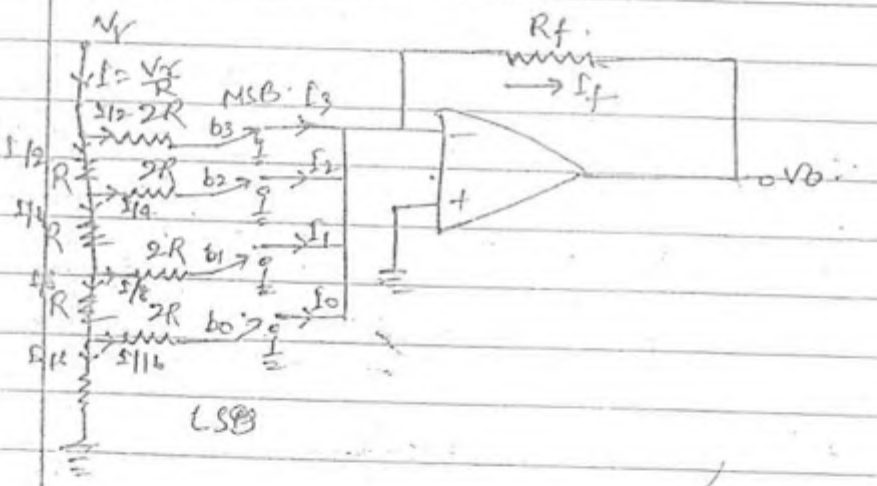
$$I_f = \frac{V_r}{2^n}\left(\sum_{i=0}^{n-1} 2^i b_i\right) \times \frac{1}{R_1+R}$$

P-49 Q.2.2

$$I_0 = \frac{V}{8/4} \times \frac{2}{3} \times \frac{1}{3R} = \frac{V}{R}$$

3bit

☆ Inverted Ladder DAC :→



→ Switch is always ground potential.

→ There is no charging or discharging.

$$I_3 = \frac{I}{2} \times b_3 \qquad I_1 = \frac{I}{8} \times b_1$$

$$I_2 = \frac{I}{4} \times b_2 \qquad I_0 = \frac{I}{16} \times b_0$$

$$\boxed{I_f = I_3 + I_2 + I_1 + I_0}$$

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$$I_f = \frac{1}{2} b_3 + \frac{1}{4} b_2 + \frac{1}{8} b_1 + \frac{1}{16} b_0$$

$$= \frac{1}{16} [8b_3 + 4b_2 + 2b_1 + b_0]$$

$$I_f = \frac{1}{2^n} \sum_{i=0}^{n-1} 2^i b_i$$

$$\left[I_f = \frac{V_r}{2^n} \sum_{i=0}^{n-1} 2^i b_i \cdot \frac{1}{R} \right] \quad \left[\because I = \frac{V_r}{R} \right]$$

$$\left[V_0 = \frac{V_r}{2^n} \sum_{i=0}^{n-1} 2^i b_i \left[-\frac{R_f}{R} \right] \right]$$

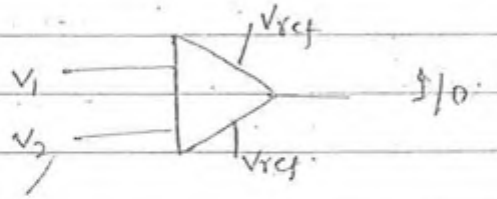
W·B Q5 Wkt 20

$$V_0 = \frac{10}{16} \times 5 \times \left[-\frac{R}{R} \right] = -3.125 \qquad 0101 = 5$$

2> $V_R = \frac{4}{8} \times 2 = 1$

☆ Analog To Digital Converter :→

1> Counter Typer ADC :→

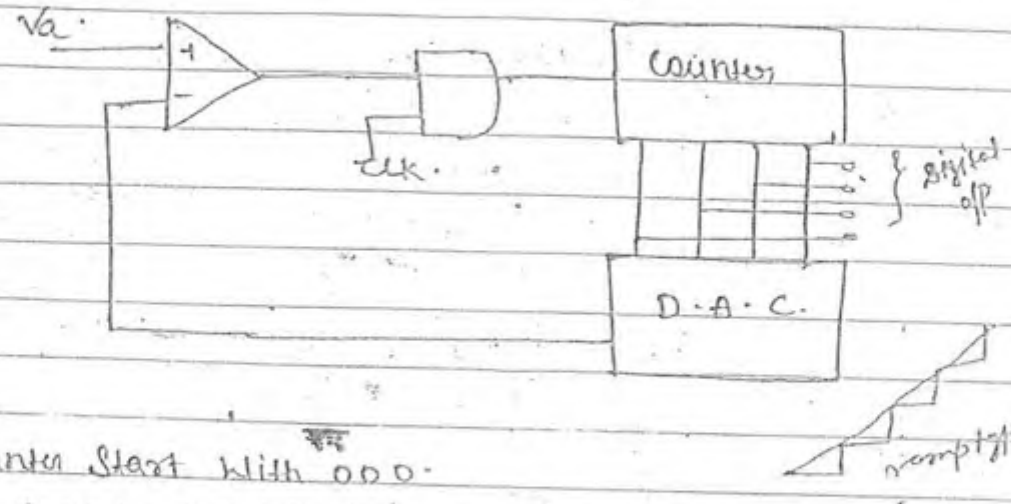


$V_1 > V_2 \rightarrow +V_{ref} \rightarrow 1$

$V_1 < V_2 \rightarrow -V_{ref} \rightarrow 0$

W·B 7> (a)

8>



→ Counter Start With 000.

→ In Counter type ADC a comparator is used at I/P stage to compare I/P Analog voltage with reference voltage provided by DAC feedback

→ A counter is used to count no. of clk pulses applied.

→ If analog voltage is greater than reference voltage then o/p of comparator of logic 1 & counter will continues clock the pulse. If Va < Vr, comparator o/p is 0 and counter will stop. At this time o/p of counter will provide binary o/p proportional to analog voltage (Va)

→ Maximum no. of clock pulses required for n-bit conversion is $2^n - 1$

→ Maximum conversion Time = $(2^n - 1) T_{clk}$.

→ Conversion time depends on I/P analog voltage.

→ Counter type ADC also known as ramp type ADC.

☆ Parallel Comparator Type :→

n bit → $2^n - 1$ Comparator

Other parts :-

2^n resistor

$2^n \times n$ priority encoder

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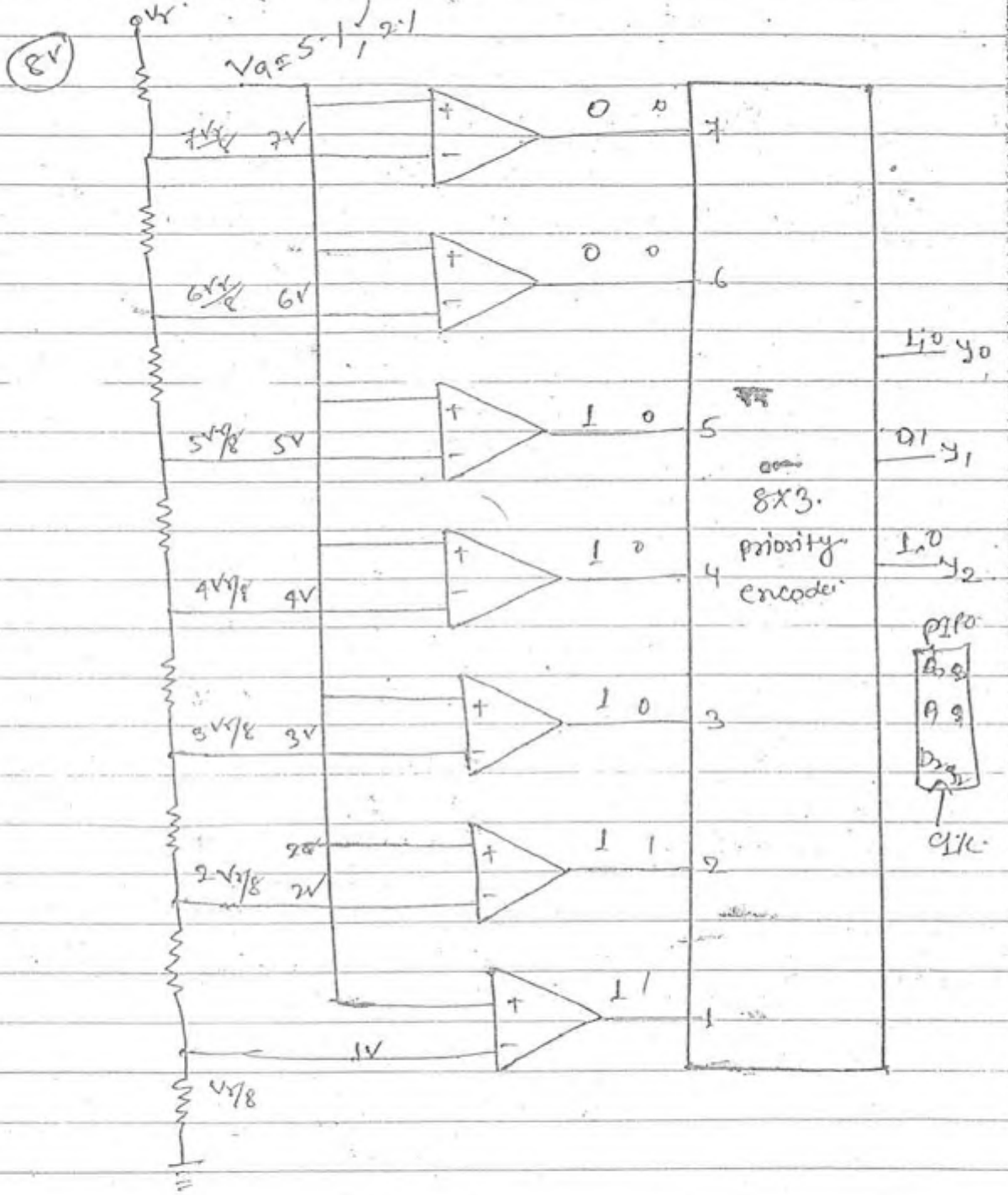
3 bit Parallel Comprator ADC :→



Parallel comprator ADC is the fastest ADC among all.
Max^m no. of clk pulse for n bit (converted) = 1 clk pulse.

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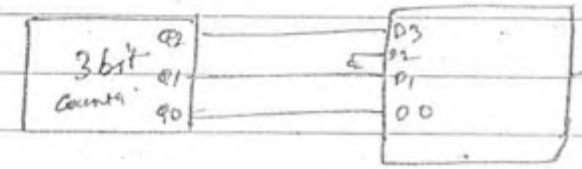
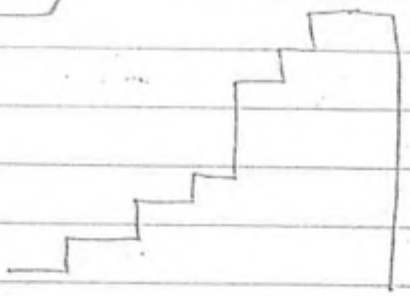
Range of Analog voltage	Binary o/p
$V_a > \frac{7V_r}{8}$	1 1 1
$\frac{6V_r}{8} < V_a < \frac{7V_r}{8}$	1 1 0
$\frac{5V_r}{8} < V_a < \frac{6V_r}{8}$	1 0 1
:	:
$V_a < \frac{V_r}{8}$	0 0 0

P 6.5 Q14



0 0 0	0 0 0 0
0 0 1	0 0 0 1
0 1 0	0 0 1 0
0 1 1	0 0 1 1
1 0 0	1 0 0 0
1 0 1	1 0 0 1
1 1 0	1 0 1 0
1 1 1	1 0 1 1



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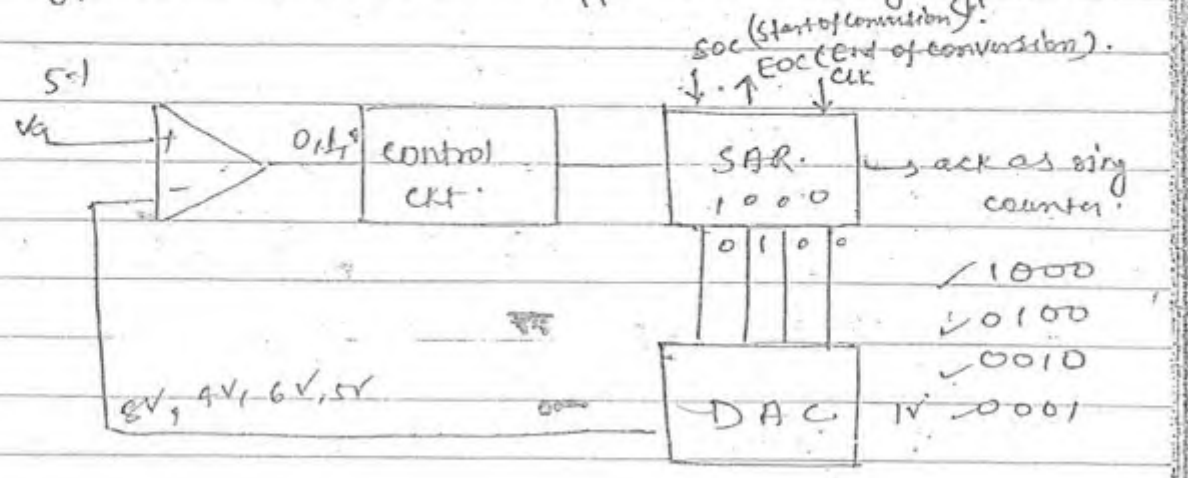
☆ ~~SAR Type ADC (Successive~~

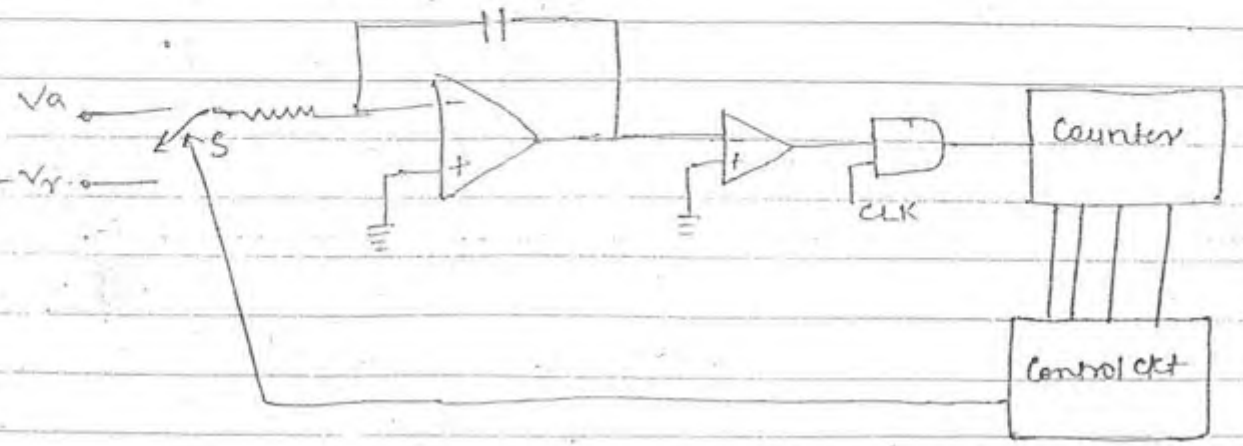
☆ SAR Type ADC (Successive approximation reg. type) :→



Ring Counter → Set
Control ckt to reset ($V_a < V_r$)

→ In SAR type ADC ring counter will present to successively to set the bit.
→ Control ckt is used to reset previously set bit when $V_a < V_r$
→ In SAR type ADC, n clk pulse required for n bit conversion.
→ Conversion time = nT_{CLK}.
→ In SAR type conversion time is uniform for any analog voltage (Independent of analog voltage)
→ Mostly used in digital ckt to provide interfacing with microprocessor.

☆ Dual Slope Integrating Type ADC :→



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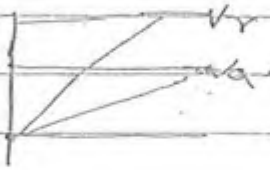
Note:-

→ $V_o = \frac{-1}{RC}\int v_i dt$

$= \frac{-V_i}{RC}\int dt$ [V_i = const]

$= \frac{-V_i \cdot t}{RC}$



→ $|V_a| < |V_r|$.]

→ In dual slope ADC a counter is used to count clk pulses.

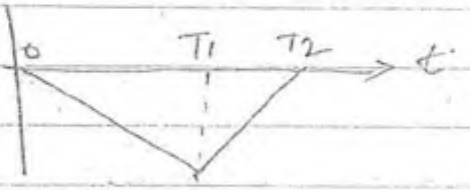
→ When conversion is started initially counter is reset to 0 and switch 'S' is connected to analog voltage V_a.

→ When integrator is integrating analog voltage o/p of integrator become -ve voltage. Due to this comparator o/p is logic 1 & counter will continues clk pulse.

→ After 2^n clk pulse again counter value becomes 0. At this time (T_1) control ckt will connect switch S to refrence voltage $-V_r$.

→ During refrence voltage integration upto T_2 time o/p of integrator is -ve voltage due to this counter will again continues clk pulse. At time T_2 o/p of integrator becomes +ve & comprator o/p will become 0 due to this counter will stop.

→ Let N is the count when counter is stop.



$T_1 = 2^n T_{clk}$.

$T_2 - T_1 = N T_{clk}$.

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$$V_o = -\frac{V_a}{RC} T_1 + \frac{V_r}{RC} (T_2 - T_1) \quad --(1)$$

At time $t = T_2$

$V_o = 0$

∴ from eqⁿ (1)

$$0 = -\frac{V_a}{RC} T_1 + \frac{V_r}{RC} (T_2 - T_1)$$

$$\frac{V_a}{RC} T_1 = \frac{V_r}{RC} (T_2 - T_1).$$

$$V_a 2^n T_{clk} = V_r N T_{clk}$$

$$\boxed{V_a = \left(\frac{V_r}{2^n}\right) N}$$

If $V_r = 2^n$

$$\boxed{V_a = N}$$

Above all ADC, dual slope ADC is most accurate

$$\boxed{\text{No. of clk pulse} = 2^n + N}$$

It is mostly used in digital voltmeter.

Maximum No. of clk $= 2^n + 2^n - 1$

$\Rightarrow 2^{n+1}$ $2^n + 2^n$.

So it is slowest ADC among all ADC.

Counter type $\rightarrow 2^n - 1$

SAR $\rightarrow n$

flash $\rightarrow 1$

Dual $\rightarrow 2^{n+1}$

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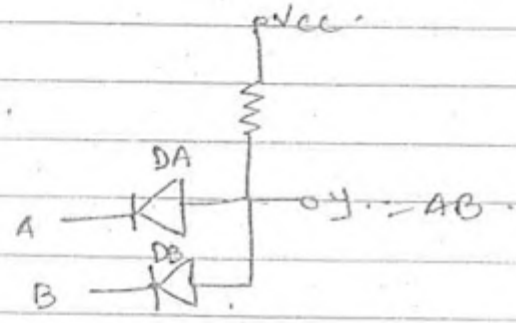
Logic families

1. DTL
2. TTL
3. ECL
4. NMOS
5. CMOS
6. RTL
7. DCTL
8. I^2L
9. HTL
10. PMOS.

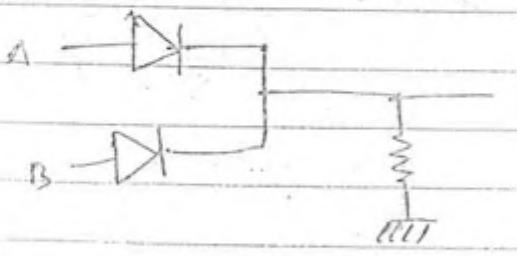
→ AND.



AND gate.

A	B	D_A	D_B	y
0	0	ON	ON	0
0	1	ON	Of	0
1	0	Off	ON	0
1	1	OFF	Of	1 (Vcc)

→ OR :-



OR gate.

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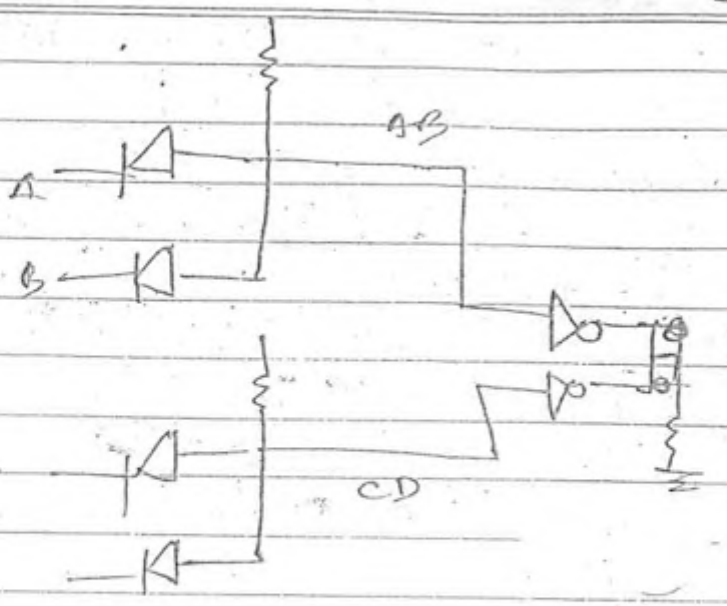
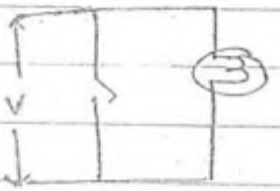
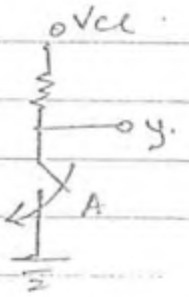
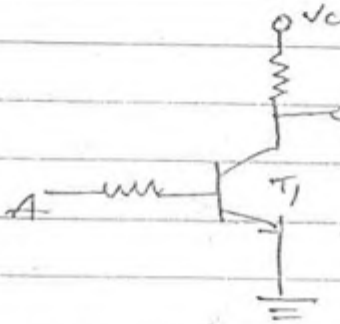


→ NOT :→



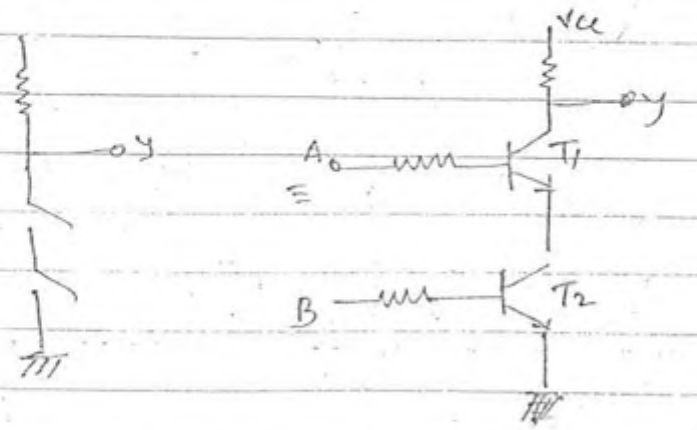




A	y
0	1
1	0

A	T_1	y.
0	OF	1
1	ON	0

→ NAND Gate :—



A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

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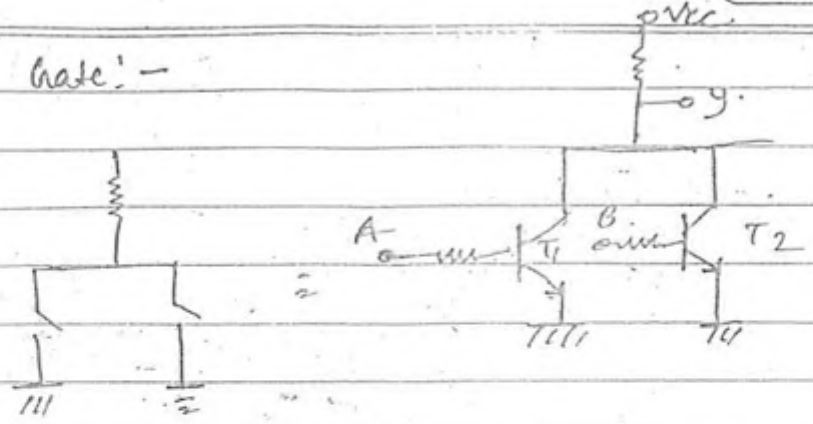
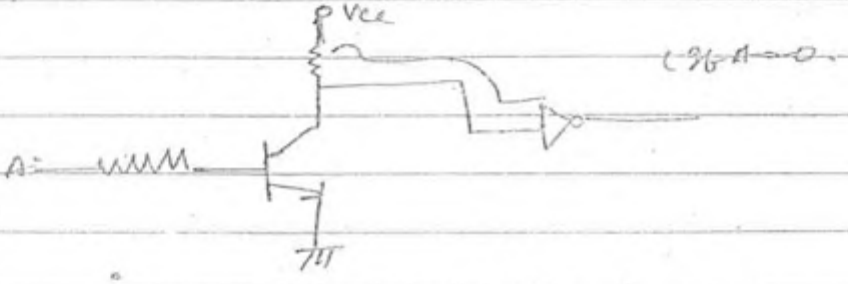
→ NOR Gate:-



A	B	T_1	T_2	y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0



→ When logic gate O/P is 1 (Tr is OFF) it will acts as current source.

→ When O/P is logic 0 (Tr is ON) it will acts as current sink.

→ Transistor:

J_{EB}	J_{CB}	
R.B	RB	Cut-off
FB	R.B	Active
RB	FB	Reverse active
FB	FB	Saturation

In Cut-off & Saturation region transistor act as a switch.

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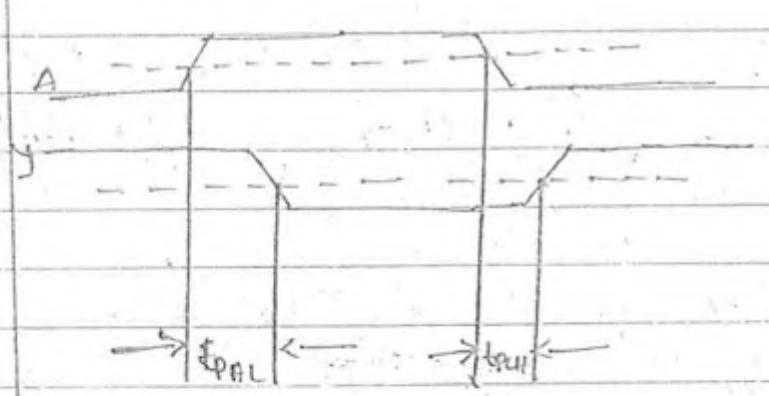
Characteristic of logic family :-

1) t_{pd}
2) P_{diss}.
3) figure of merit.
4) Fan out.
5) Noise Margin.
6) Wired logic.
7) Fan out.

1) Propagation Delay (t_{pd}) :→

It is measured in ns.



Off-ON ON-Off

In transistor ON-OFF time is more compaired to OFF-ON time due to saturation or storage time.

$$t_{p.d} = \frac{t_{pH.L} + t_{pL.H}}{2} \text{ ns.}$$

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2: Power Dissipation (Pdiss) :→

→ Power dissipation represent power dissipated per logic gate

→ Its unit is mw.

$$P_{diss} = V_{cc} \cdot I_{c\,avg}$$

3. Figure of Merit :— .

Product of propagation delay & power dissipation.

$$\text{Figure of Merit} = P_{diss} \times t_{pd}$$

mw x ns.

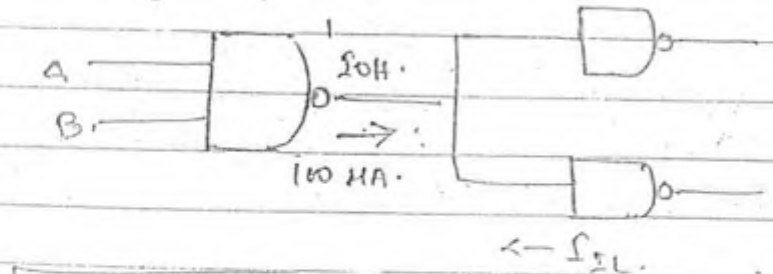
PJ.

It unit is PJ.

⁂ I^2L has best figure of merit among all logic family.

4) fan-out :→.

It is the maxm no. of logic gates that can be driven by logic o/p.



$$\text{fan out}_H = \frac{I_{OH}}{I_{IH}}$$

I_{OH} ⇒ current source.

Logic 1.

$$\text{Fan out}_L = \frac{I_{OL}}{I_{IL}}$$

current sink.

(Logic 0)

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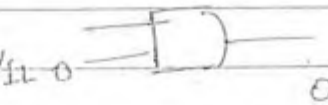
Fan out = (Fan out$_H$, Fan out$_L$) min.

Q. In TTL logic family:
$I_{OH} = 400\ \mu A$.
$I_{IH} = 40\ \mu A$.
$I_{OL} = -16\ mA$.
$I_{IL} = 1.6\ mA$.
Then fan out of logic family.

Sol: $\frac{I_{OH}}{I_{IH}} = \frac{400}{40} = 10$.

$\frac{I_{OL}}{I_{IL}} = \frac{16mA}{1.6} = 10$.

5) Noise Margin :→
It is the maximum noise voltage that can be added to a logic family which will not affect the o/p.



$$V_{OH} > V_{IH} > V_{IL} > V_{OL}$$

$$NM_H = V_{OH} - V_{IH}.$$

$$NM_L = V_{IL} - V_{OL}$$

$$NM = (NM_L, NM_H)_{min}$$

W.B 1.(D) 11) $V_{OH} = 3.8$] 0.7V → NM_H
$V_{IH} = 3.1V$
$V_{IL} = 2.0$] = 1.3V NM_L
$V_{OL} = 0.7$

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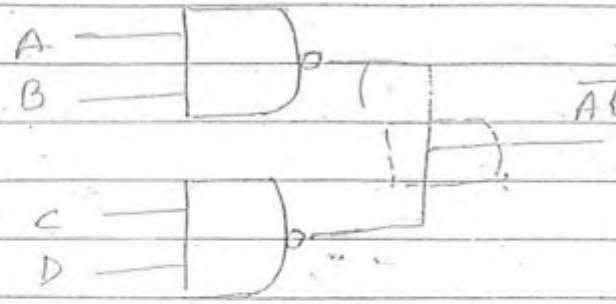
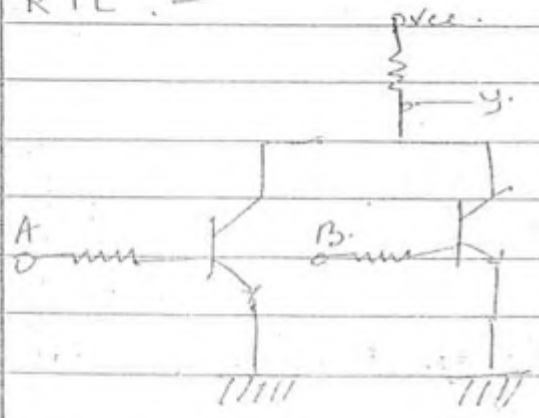
6) Wired logic :-



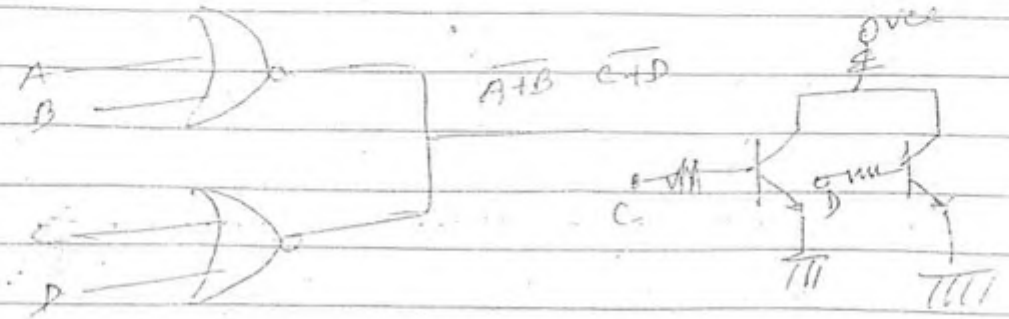
[Wired AND]

* RTL :-



1) Basic gate :→ NOR
2) tpd = 50 ns.
3) Pdiss = 10 mW
4) figure of Merit = 500 P.J.
5) NM = 0.2 V
6) fanout = 3
7) Wired AND

8)



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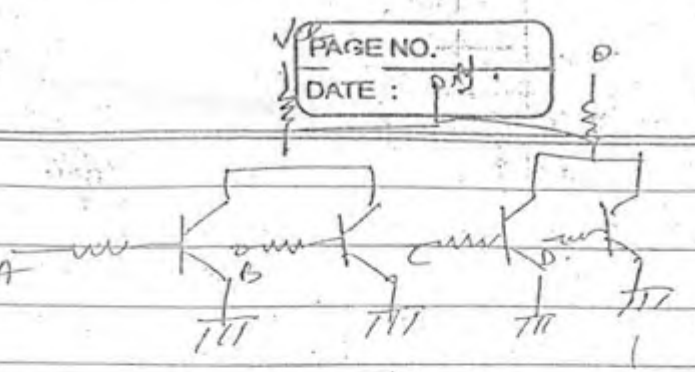
A	B	C	D	Y
0	0	0	0	1
0	0	1	0	0
0	0	1	1	0

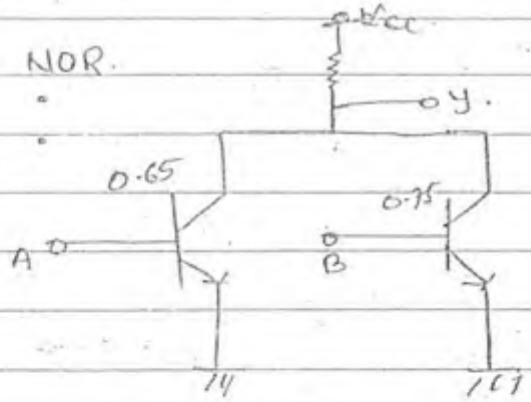


Disadvantages of RTL :→
Low Speed of operation.
Lower fan out
Low noise margin.

* DCTL (Direct Coupled Transitor logic) :—
In RTL logic family if I/P resistor are removed then the resulting logic family is DCTL

→ tpd = 40ns

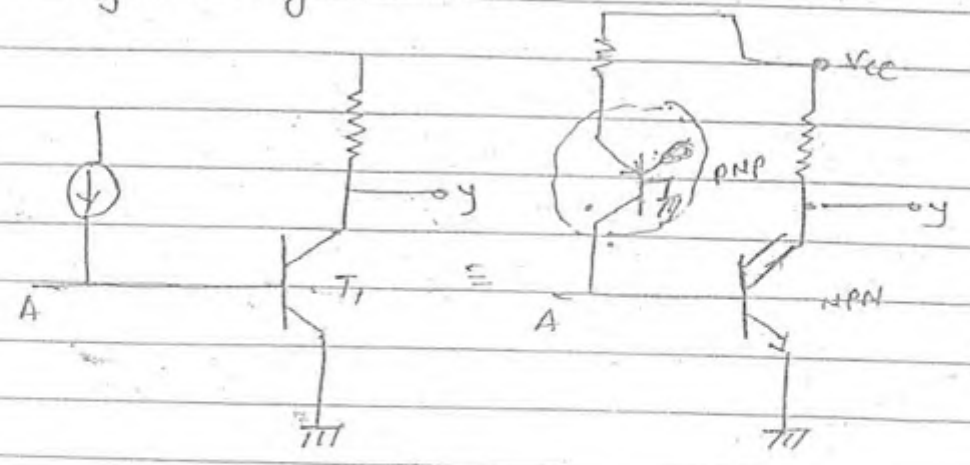
→ Basic gate → NOR.



A	B	T_1	T_2	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	OFF	0

Disadvantage :-
→ Current fogging
In DCTL logic family if Tr with different characteristic are used the Tr have lower V_{BE}sat first become ON when it will not allow other Tr to ON. This is known as current fogging

✡ Integrated Injection logic (I^2L) :→



A	T_1	y.
0	OFF	1
1	ON	0

→ Fan out = 8 (due to multiple character)
→ tpd = 40ns.
→ figure of Merit = 0.1PJ – 0.7PJ.
→ Gate.

SSI	1 to 12
MSI	13 to 99
LSI	100 – 1000
VLSI	> 1000

→ In I^2L logic family due to integration of PNP & NPN tr it occupies less area. hence densities are more
→ It is mostly used in MSI & LSI logic family
→ Due to use of multi character o/p fan out is increased.

✡ MTL (Merged Transistor logic) – other name.

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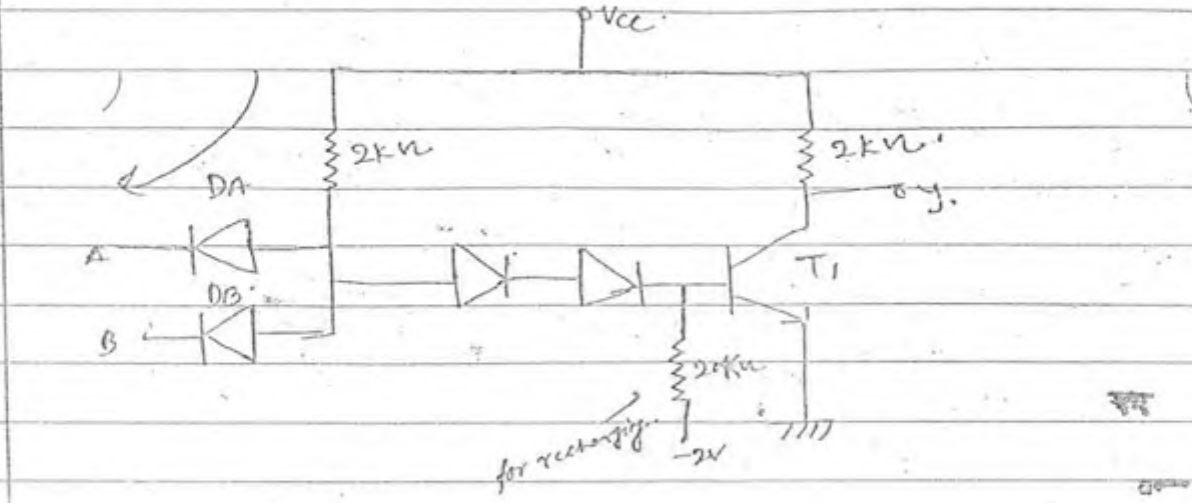
✱ DTL (Diode Transistor logic family) :→



A	B	T_1	Y
0	0	OFF	1
0	1	OFF	1
1	0	OFF	1
1	1	ON	0

→ Operation :-

The ckt shown in fig is known as basic DTL gate. In this any I/P is low or all the I/P are low, Diode DA and DB will become forward bias when as D_1 & D_2 will become reverse bias due to this Tr T_1 is off & O/P is 1.

When all the I/Ps as high DA & DB will become reverse bias & D_1 & D_2 will become forward bias & Tr T_1 is ON & O/P is low.

→ Basic gate - NAND
→ t_{pd} = 30ns.
→ P_{diss} = 8mw
→ Figure of Merit = 240 PJ
→ Noise Margin = 0.75 V

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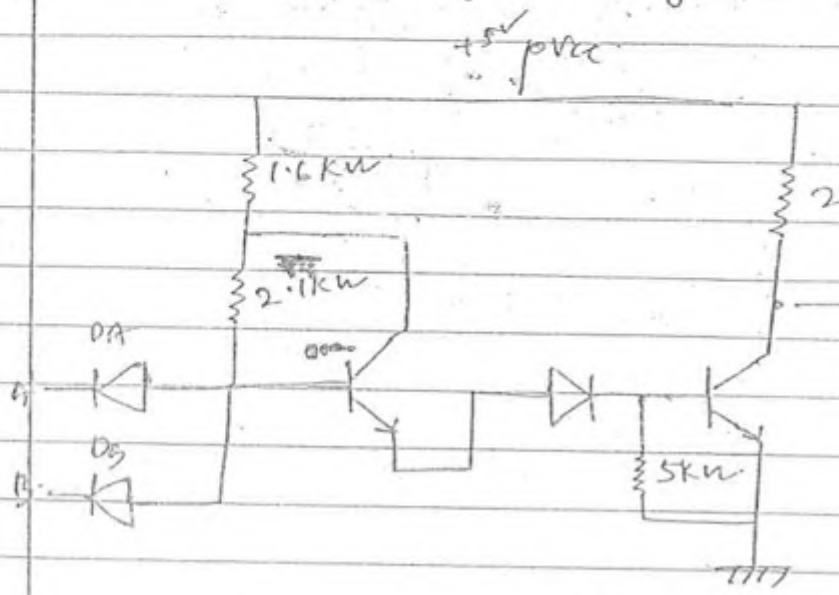
→ Fan out = 3 (low)

→ Wired AND

☆ Standered Diode Transistor logic

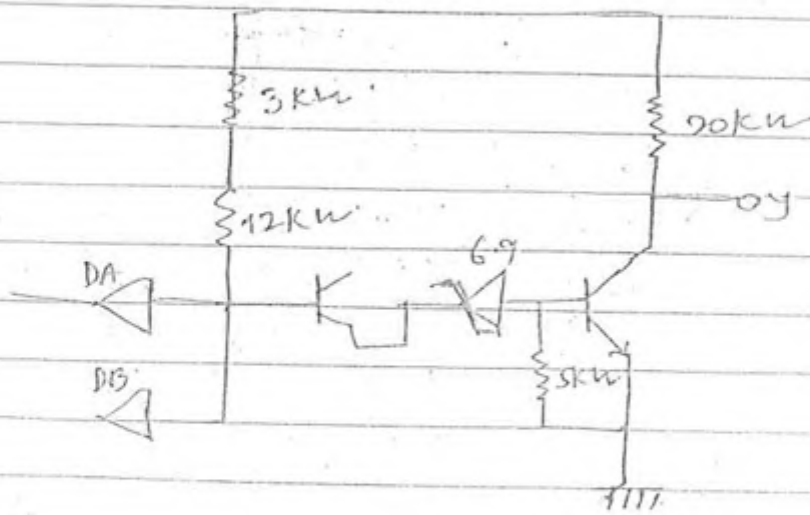


$P_n = KTB.$

$V_n = \sqrt{4KTBR}$

Fan out = 8

☆ High Threshold logic family (HTL) :-



Advantage

i) Noise margin → 4-5 V ☆ (highest)

logic

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ii) logic 0 = 2V
logic 1 = 12V

iii) Higher voltage Swing

iv) t_{pd} = 90 ns.

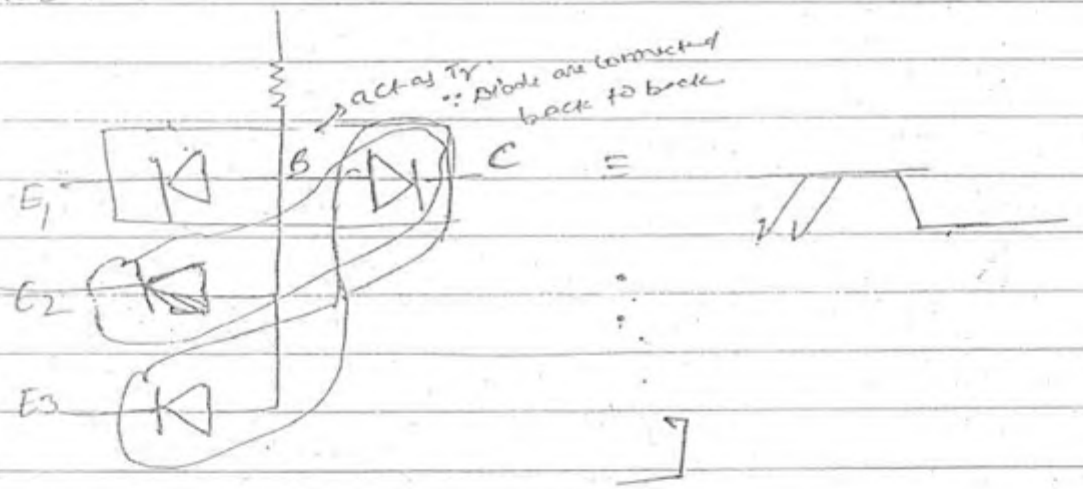
v) Power dissipation = 55 mW

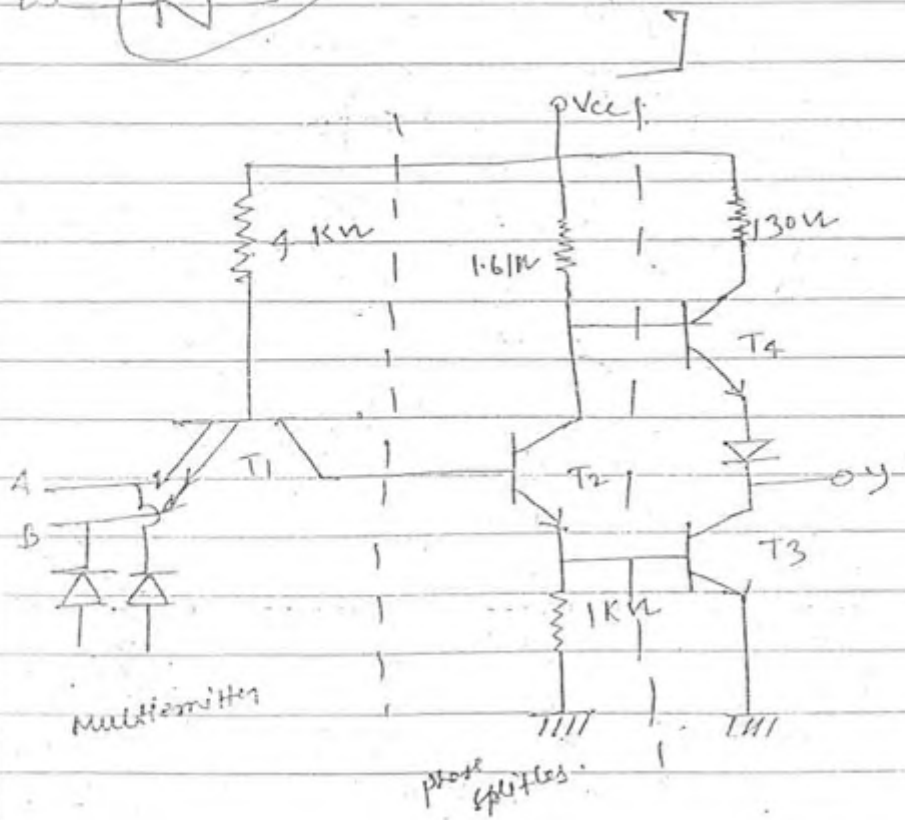
vi) Figure of Merit ≈ 5000 PJ.

vii) Fan-out = 10

☆ Transistor Transistor logic family (TTL) :→

[Note:—





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A	B	T_1	T_2	T_3	T_4	Y.
0	0	A	c	c	s	1
0	1	A	c	c	s	1
1	0	A	c	c	s	1
1	1	R	s	s	c	0

The CKt shown in fig. is standered TTL. It basically have three states.

1) Multi Emitter I/P stage.
2) Phase splitter
3) Totem pole o/p stage or ACtive pulling o/p stage.

Operations:-

In this any I/P are low or all the I/Ps are low then Emitter base junction of T_1 is forward biased & collector base junction of T_1 is reversed biase (T_r. is in active mode)

Due to this T_{r2} & T_{r3} is OFF where as T_{r4} is in saturation hence o/p is 1.

When all the I/P are high then EB junction of T_1 is reversed biased where as C-B junction is forward biased (Mode → Reverse active)

Due to this T_2 & T_3 are in saturation T_4 is in cut-off hence o/p is zero.

$V_{IH} = 2.0$ V

$V_{OH} = 2.4$ V

$V_{IL} = 0.8$

$V_{OL} = 0.4$

i) Fan out = 10

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ii) t_{pd} = 10 ns

iii) P_{diss} = 10 mW

iv) Figure of merit = 100 PJ

v) Noise Margin = 0.4 V

8) (b)

→ Diode D is used to Cut-off T_{P4} when T_{P3} is ON

→ Advantage of Totem pole.

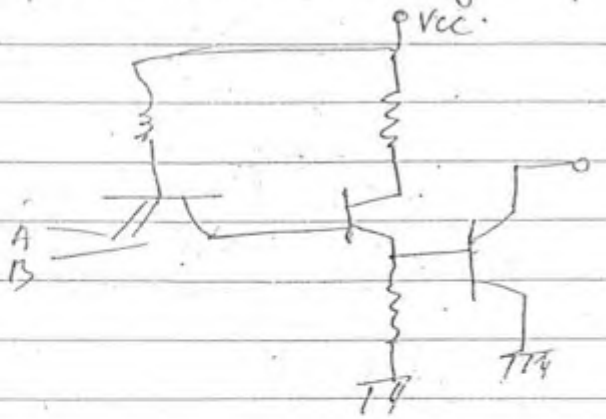
i) Lower P_{diss}.

ii) Highest speed of operation & higher fanout.

Disadvantages:-

i) It is not used in Wired Logic.

→ To provide Wired AND logic open collector configuration is used.



W.B 9 (a)

→ 130 Ω Resistor is used in collector load of o/p stage in o/p stage to reduced ripple or generation of high freq. operation.

→ Clamping diodes are connected at o/p stage to protect T_3 during high freq. of operation (ringing)

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☆ Different types of TTL :→

1) Standered TTL
2) High Speed
3) Low power
4) Schottky TTL.

2) High Speed TTL :—

In Standered TTL logic family if resistor values are reduced the propagation delay will reduce, then the resulting logic family is known as high speed TTL.

$t_{pd} = 6$ ns.

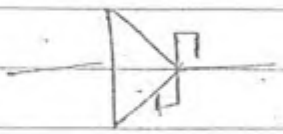
→ Disadvantages:-

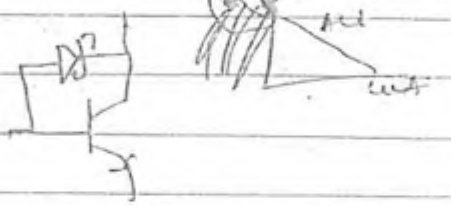
Pdissipation is increase.

3) Low Power TTL :—

In TTL Logic family if resistor values are increased then Pdiss is reduced & resulting logic family is known as low power TTL.

4) Shottkey TTL :—





If Shottkey diode is used b/w C-B region then it will remove storage time or Saturation delay resultant logic family is know as Shottky TTL

$t_{pd} = 2$ ns.

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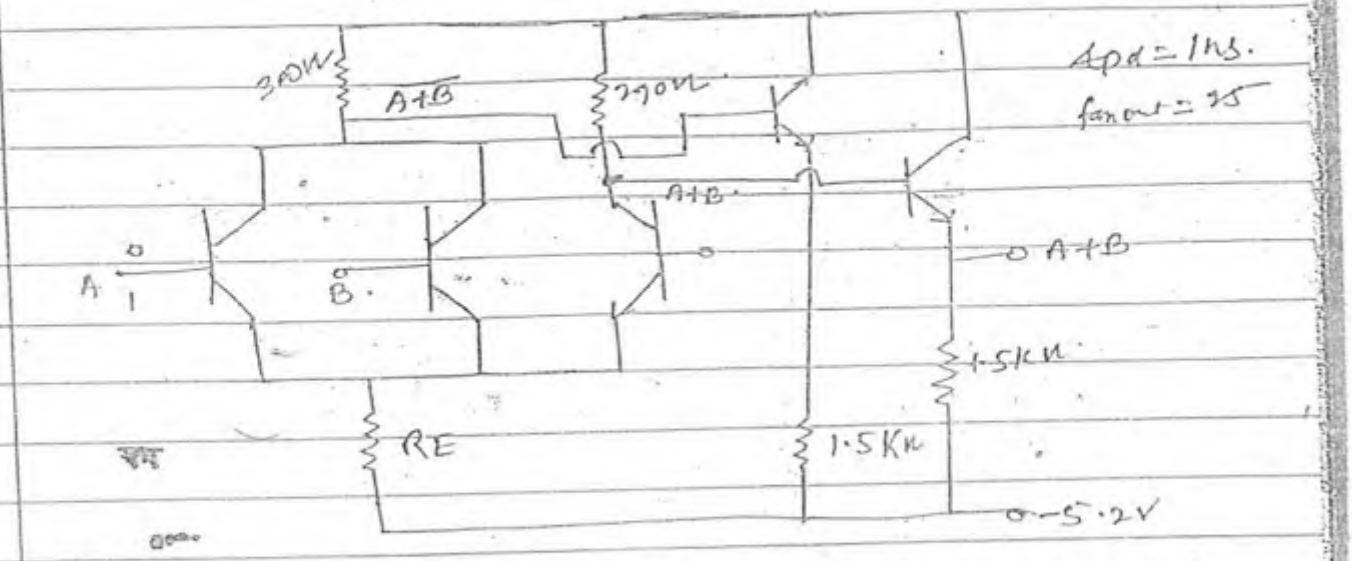
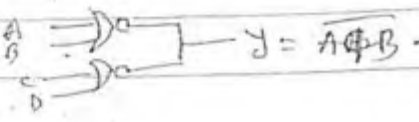
☆ Emitter Coupled Logic Family [ECL] :→



i) It is the fastest logic family because it is non saturated logic family.
ii) In this Tr is operated in cut-off & active mode.
iii) It basically contain two stage
A) Differential Amplifier I/P stage.
B) Common collector emitter follower O/P stage.
iv) Due to use of differential amplifier complement O/P are available in ECL family (NOR or OR gate)
v) Due to use C-C stage in the I/P fan out is also high.
vi) ECL logic family uses -ve power supply due to this any power supply, spikes, blicks will not effect.
vii) Pdis = 50mW.
viii) tpd = 1ns.
ix) Figure of Merit = 55 PJ.
x) fan out = 25
xi) Noise Margin = 0.3V
xii) Logic 0 → -1.7V
1 → -0.85V.
xiii) It will provide wired OR gate.



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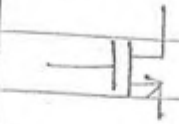
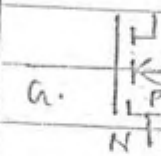
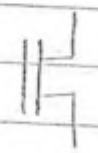
NMOS :→

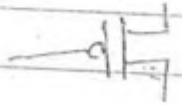




	Tr	PMOS.
G.	0V →	OFF ON
	ON	OFF

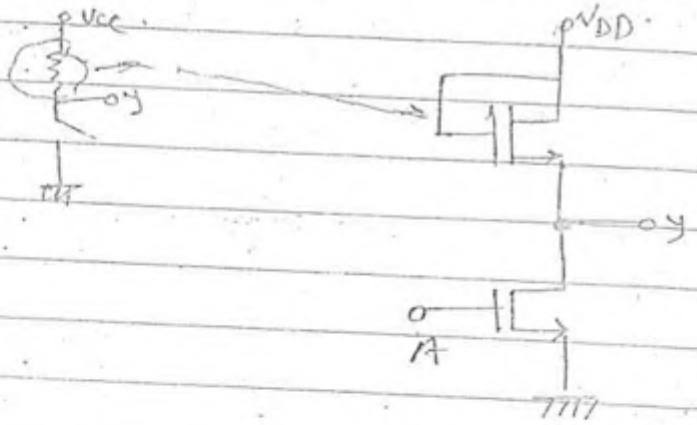
In n-channel MOSFET logic 0 it is OFF & logic 1 it is ON
In P-channel MOSFET logic 0 it is ON & logic 1 it is OFF.


NMOS.


PMOS.

→ ~~NMOS~~ :

NOT:- (NMOS NOT)



A	T2	Y.
0	OFF	1.
1	ON	0'

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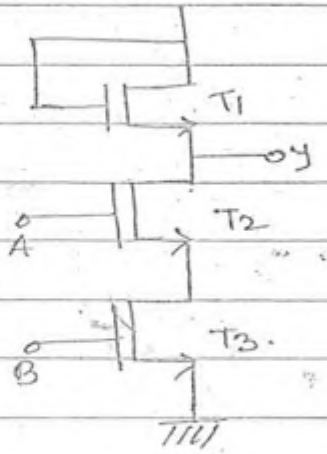
→ NMOS NAND.



A	B	T_2	T_3	Y.
0	0	Off	Off	1
0	1	Off	ON	1
1	0	ON	Of	1
1	1	ON	ON	0

Q.B10> (a) 9> $\overline{A(B+C)+DE}$

→ tpd = 250 nS.

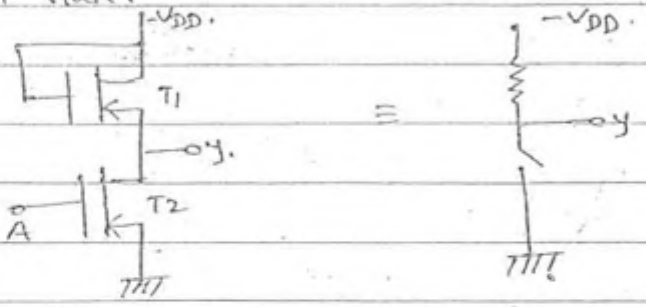
→ Pdiss = 100 W

→ figure of Merit = 250 PJ.

→ fan out = 5

→ Noise Margin = 1.5 V

☆ PMOS NOT Gate: →



A	T_2	O/P voltage	Y
0	ON	GND.	1
1	OFF	$-V_{DD}$	0

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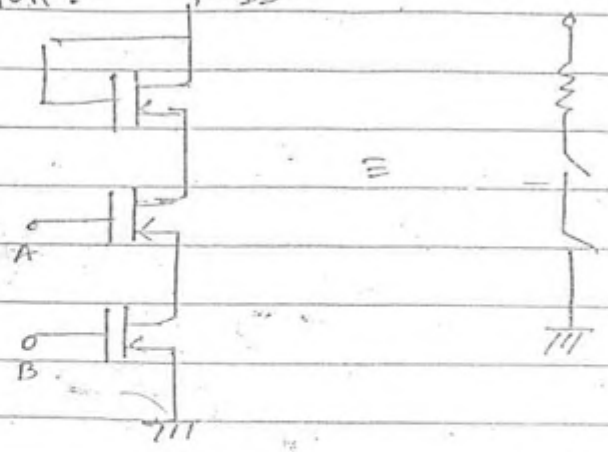
→ PMOS NOR :→ $\phi - V_{DD}$.



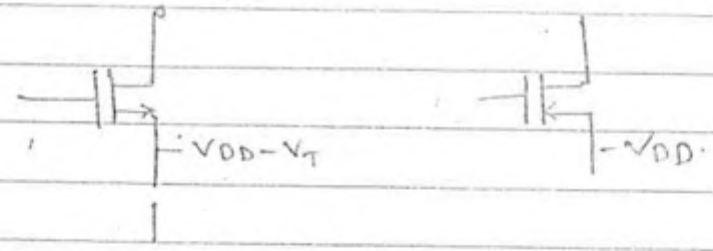
A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

t_{pd} = 300ns.

P_{dis} = 0.2 mW

'Figure of Merit' = 60 PJ.

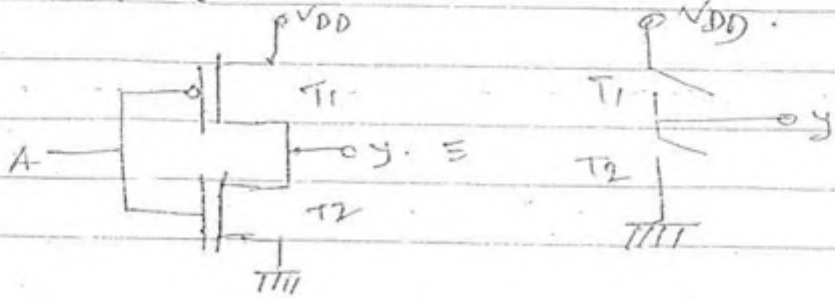
☆ CMOS



PMOS → Strong → 1.
→ Weak → 0

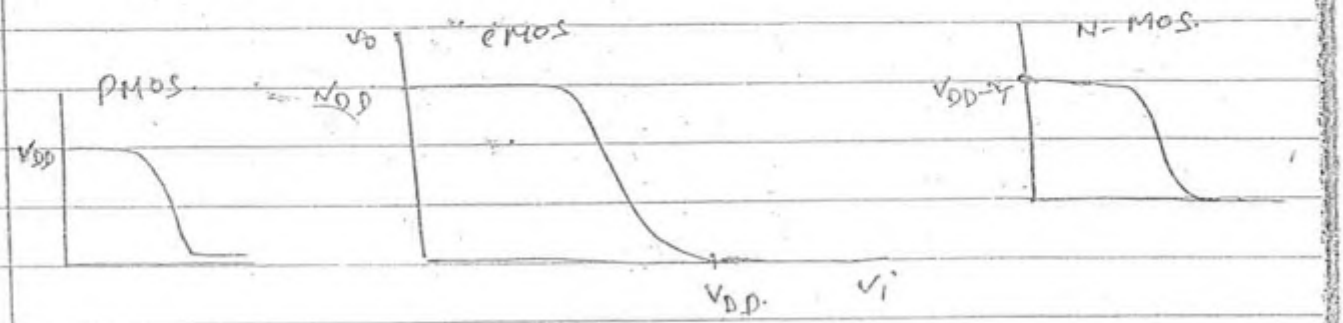
NMOS → Strong → 0
→ Weak → 1

→ CMOS NOT :→



A	T_1	T_2	Y
0	ON	OFF	1
1	OFF	ON	0

→ Transfer characteristic :-



Advantages

Lowest Power dissipation.

$P_{diss} = 0.01\ mW$ (Station)

$t_{pd} = 870ns$.

Figure of Merit = 0.7 PJ.

fan out = 50. (highest)

Noise Margin = $\frac{V_{DD}}{2}$ (good)

→ Power dissipation :-

1 Static → During logic 0 or logic 1.

2) Dynamic → 0 → 1 or 1 → 0

$\propto C \cdot f^2 \cdot V_{DD}^2$

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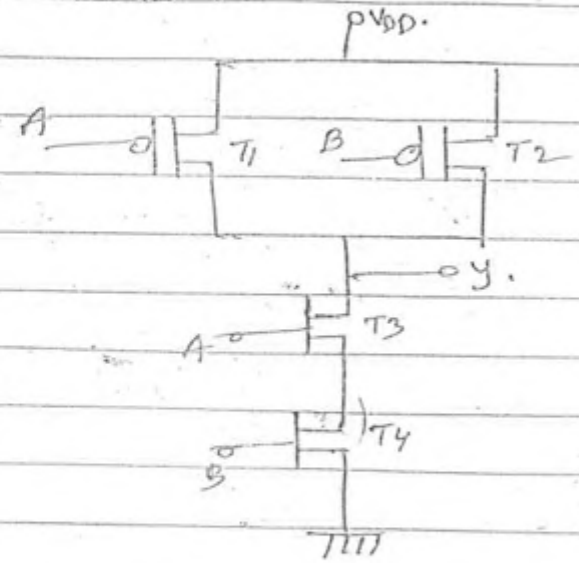
→ CMOS NAND :—



A	B	T_1	T_2	T_3	T_4	y
0	0	ON	ON	OFF	OF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

10.B1) (b)

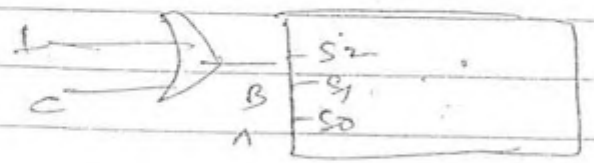
i) CMOS. → $V_{DD}/2$

ii) DTC. — 0.75V

iii) RTL — 0.2V

iv) ECL — 0.3V

9) (b)



S_2	S_1	S_0		
A	B	A		
1	0	0	x_4	0
1	0	1	x_5	1
1	1	0	x_6	1
1	1	1	x_7	0

A ⊕ B.

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☆ Binary To Gray Code Conversion :→

✳ Gray Code :→

→ Gray code is unweighted code.

→ Successive no. will differ by only 1 bit.

→ unidistance code (UDC)

→ Cyclic

→ Reflective.

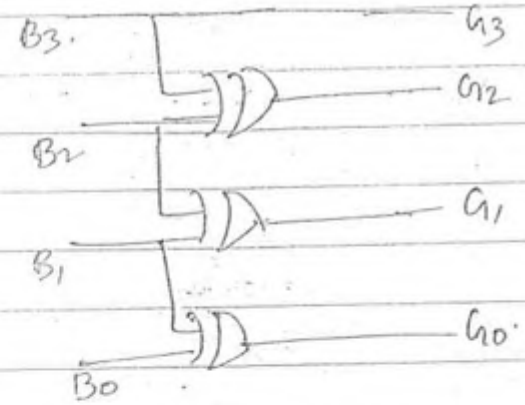
→ Minimum error code.

B_3 B_2 B_1 B_0

1 0 1 1

1 1 1 0

G_3 G_2 G_1 G_0



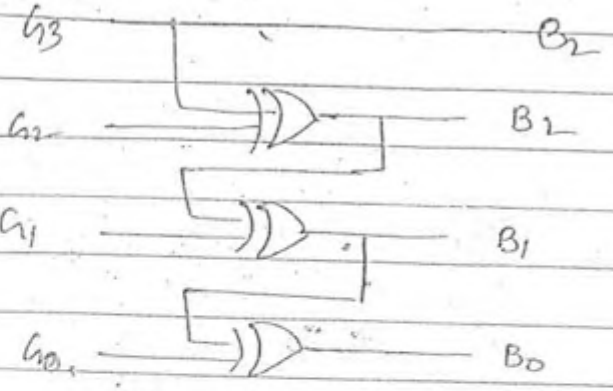
☆ Gray To Binary Conversion →

G_3 G_2 G_1 G_0

1 1 1 0

1 0 1 1

B_3 B_2 B_1 B_0



Data Representation.

- Magnitude
  - Signed → +ve → No sign bit
  - unsigned → +ve, -ve
- Complement
  - 1's → +ve, -ve
  - 2's → +ve, -ve.

One extra bit → Sign.
Sign → MSB.
MSB → 0 → +ve.
MSB → 1 → -ve.

Ex :-

+6

110	0110	0110	0110

-6

X	1110	1001	1010

→ In all representation +ve no. are represented in a similar way.
→ To represent -ve no. in sign magnitude only sign bit is changed.
→ In 1's complement, to represent -ve no, first write +ve no then 1's complement

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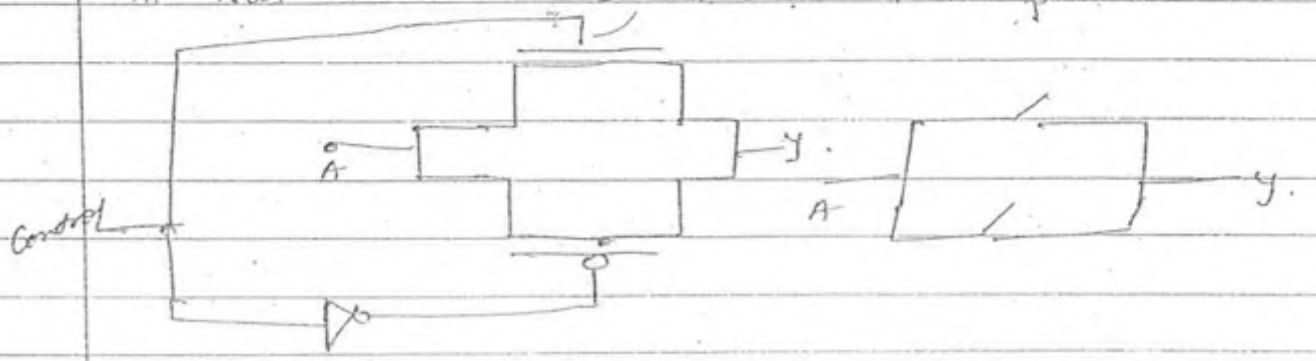
5 (d)
6 (a)
12 (d)
14) (d)
15 a

☆ Transmission Gate :→

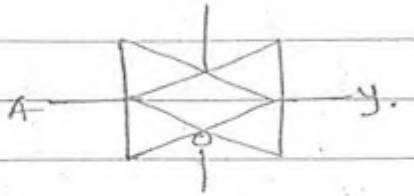
9☆ this NMOS & PMOS are connected in parallel.



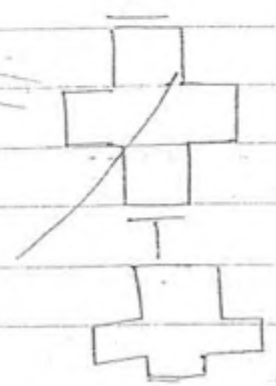
control	A	Y.
0	X	High impedence.
1	0	0
1	1	1

control	Y
0	High
1	A

Symbol :-



2 : 1 Mux :→



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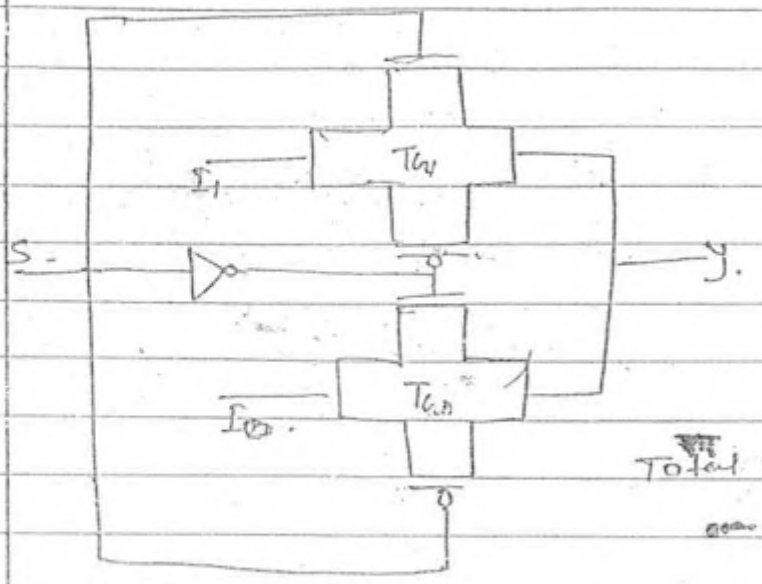
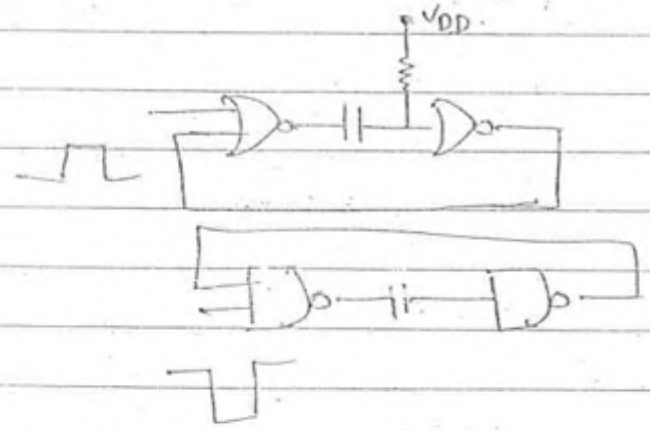
→ 2:1 MUX using Transmission Gate:—



Total no. of Tr = 2+2+2 = 6

S	y.
0	I_0.
1	I_1

→ CMOS NOR gate Monostable Multivibrator:—



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→ In 2's complement to represent -ve no. first write +ve no. then complement to each (2's complement)

→ A no is represent in 2's complement fo 011 the eq- decimal no

1011 = 1101

= -5.

Ans (d) 10011

-(01101)

-13.

(10) (a) -127 → 1's → n

→ 2's → m

127 → 01111111

1's comp -127 → 10000000 · n=1

2's -127 10000001 m=2

m : n = 2 : 1

→ (4) 5-4

5+(-4)

+5 → 0101

-4 → 1100

0001

(1) (A)

+4 → 0100

-4 → 1100

In 2's addition if any carry is present it is discar.

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17 1001 ← -7
11001 = -7
(11001 = 7.
(11001

→ In 2's complement to extend no. of bit copy MSB bit.

	Binary	Sign Mag.	1's	2's
0	0000	+0	+0	+0
1	0001	+1	+1	+1
2	0010	+2.	+2	+2
3	0011			
4	0100			
5	0101			
6	0110			
7	0111			
8	1000	-0	-7	-8
9	1001	-1	-6	-7
10	1010			
11	1011			
12	1100			
13	1101			
14	1110	-6	-1	-2
15	1111	-7	-0	-1

Range with sign magnitude.
4 bit
Sign mg → -7 to +7
1's → -7 to +7.
2's → -8 to +7.

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→ Sign magnitude, 1's.

n bit → $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$.

$-(2^{4-1}-1)$ to $+(2^{4-1}-1)$

-7 to $+7$.

WB 6 (a) 19

$X = 01110$

$Y = 11001$

00111 ①

$0\ 00111$

From copy done

→ +5, +4 using 2's complement

+5 → 0101

+4 → 0100

1001

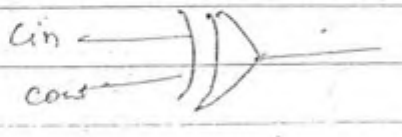
Cout=0 overflow. Cin=1

Overflow may occur when two same sign are added in signed representation.

Let X and Y are sign bits of two no. & Z is the resultan sign no. Then condition for overflow is

$$\bar{X}\bar{Y}Z + XY\bar{Z}$$

Let Cin is carry into the MSB & Cout is carry from MSB. Then



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Memories.

- Primary
  - RAM
    1) R/W
    2) Random access. (same time)
    3) Volatile
    4) Storage of Temporary data
  - ROM
    1) Read only.
    2) Random access
    3) Non volatile.
    4) Storage of Permanent data.
    Ex BIOS / System prog.
- Secondary
  - Semirandom
    1) All discs.
    2) CD
    3) DVD
    4) H.D.
  - Serial access
    1) Magnetic type.
    2) Magnetic bubble
    3) Ferrite core.
    4) C.C.D. → Charged coupled device

→ Ferrite Core → DRO

☆ Ist RAM :→

→ With n bit address, max^m no. of Mem location required = 2^n.

→ In each memory location small m no. of bits are stored then memory capacity is $2^n \times m$.

Ex

4K × 8

$2^{\frac{1}{2}}$ $2^{\frac{1}{4}}$ 10. → Data.

2^{12}.

In 4K×8

12 = Address line.

8 → Data line.

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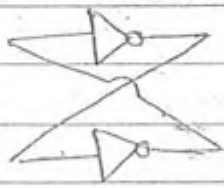
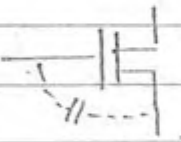
RAM

Static RAM	Dynamic RAM
1) Stored like F.F. 	1) Data stored in MOS Capacitor. 2) MOSFET 
2) ~~BJT~~ MOSFET	3) Slower
3) Faster	4) Less Power
4) Power dissipation more.	5) Higher Densities.
5) Densities less.	6) Main memory.
6) Cache memory.	7) Refreshing is required.
7) No Refreshing	

↓

→ M/c understandable Code.

DIGITAL-ELECTRONICS